International Journal of Early Childhood Special Education (INT-JECSE)
DOI:10.48047/intjecse/v13i2.21280 ISSN: 1308-5581 Vol 13, Issue 02 2021

ENHANCED 12T MEMORY CELL DESIGN FOR AEROSPACE APPLICATIONS IN NANO SCALE CMOS TECHNOLOGY

[1]MD ALI HIMAYATH SWAMSHI,[2]BILLA RANJITH KUMAR,[3]SHASHIDHAR MAHESHWARAM,
[4]AMANCHA SHYAM SUNDER,[5]AMGOTH GANESH
[13]Associate Professor, [2]Assistant Professor,[45]Students
Department of ECE
Vaagdevi College of Engineering, Warangal, Telangana

***Abstract*—**As technology develops, semiconductors' sizes and separations are getting smaller by the day. Therefore, as the fundamental charge of the fragile nodes drops, SRAM cells used in aerospace applications are more vulnerable to soft-error. If a radiation particle strikes a sensitive node in a standard 6T SRAM cell, single-event upsets (SEUs) might result in data inversion. This research suggests a Soft-Error-Aware Read-Stability-Enhanced Low-Power 12T (SARP12T) SRAM cell to mitigate the effects of SEUs. The performance of SARP12T is compared to that of other recently introduced soft-error-aware SRAM cells, including RHD12T, RHPD12T, QUCCE12T, QUATRO12T, and RSP14T. The data could be retrieved even if a radiation assault flips the values of the vulnerable nodes in SARP12T. SARP12T can withstand single-event multi-node upsets (SEMNUs) caused by storage node pairs. During read operation, the bitline provides easy access to the '0' storing memory nodes in the proposed cell, which are also very resilient to disruptions. In terms of energy usage, SARP12T is likewise the most effective holding technique. When it comes to write performance, SARP12T performs better than rival cells, and its write latency is significantly shorter. All of these benefits are obtained by the proposed cell with just a little increase in read/write energy and read latency.

Keywords—Aerospace, SARP12T, QUCCE12T, SRAM

I. Introduction

Electrical infrastructure may be damaged or destroyed by the powerful ionising action of radiation in space and close to nuclear reactors. Circuit failures, particularly in data storage systems, have been connected to ionising radiation. When many radiation ionising effects occur simultaneously, the scientific community refers to this phenomenon as a "single event upset" (SEU) [1, 2]. On the one hand, it would seem plausible that long-term memory is unaffected by this radiation. The "single event multi-upset effect" (SEMU) is a phenomena that can lead to an electronic device malfunctioning when many events happen simultaneously [22]. Radiation dangers may be decreased by resetting [7] the electrical cycle using software that uses state machines to identify previous states. This reality cannot be changed by a small investment in space-related applications [4]. A soft error is caused by bit flipping in ionising CMOS [16] memory [17]. The oxide layer's pore expansion is the cause of this effect. This approach makes accessing data storage extremely slow. To further illustrate the results, it might be useful to employ a write cycle with varying length and complexity when assessing SRAM memory in the presence of ionising radiation. With each new technological generation, integrated circuit machines get smaller and more potent. Using integrated circuits, this method aims to maximise output by cramming as many parts into a limited area as is practical. Transistors, the essential components of memory cells, have grown in size as Moore's law has been generally adhered to. Therefore, it seems sense that with each generation that follows, cell density will progressively decline [1]. Each every cell is a nanoscale system because modern technology uses transistors that are so small; this is how SRAM-compatible metal-oxide-semiconductor (CMOS) memory is made. SRAM chips can therefore operate at gradually lowering voltages. This tendency has already reversed, contrary to the International Technological Strategy for Semiconductors' (ITRS) prediction that it would. The leakage current remained within an acceptable range due to the transistor's threshold voltage scaling constraint [2]. Many modern electronic gadgets rely on these static random access memory (SRAMs) to function. The provision of specialised space has played a significant role in meeting this requirement. As the expected number of patients surpasses 90%, costs are expected to rise [3]. As many SRAM cells as possible are being crammed into each component by the technicians. This process is essential for advancing the science since it produces smaller cells. Transistors in SRAMs are often located as high up in the design and as compact as is practical. To lessen the load on the electrical system, the voltage is also kept low. In actuality, though, the lower power consumption was only partially accomplished. SRAM devices have gotten smaller and need less power as a result of new technologies, but the design still faces

two major challenges: transient event radiation and cell stability. The latter phenomena is the subject of this investigation. But there are also investigations into issues with SRAM reliability. SRAMs are essential for regional radiation. Single-event upsets (SEUs), which are caused by a single energy particle, might seriously harm them. Because they do not cause lasting damage to the circuit, these failures are classified as soft errors (SE). Electron-hole pairs (SEUs), which are released when heavy particles collide, are collected in a sensitive area and used to regulate the power supply of the circuit. If there is sufficient noise, a node in an SRAM array may examine the condition of a cell and alter the data it contains. These statements are completely untrue. A passing particle might corrupt the data in one or more SRAM cells.

I. PROPOSEDMETHOD

This novel radiation-hardened-by-design (RHBD)12T storage facility features aneasily implementable layout-topology and also takes into consideration the physicalmechanism of upset in soft faults. The validation results show that the proposed 12Tcell can provide significant radiation resistance. The predicted 12T cell requires moreroom, energy, and time to read and writethana13Tcell.The986.2mVmarginofstaticnoise in the hold is more than what a 13T cell can achieve. The error-correcting capabilities of the recommended 12T cellmakeitmoretrustworthy.Thesedays,CMOStechnology is ubiquitous in the electronics sector. The aircraft industry is another thatbenefitsgreatlyfrom CMOStechnology.Memoriesaretheprimary datastoragemechanisminmanyaeronauticalapplications.CMOStechnologyisusedintheproduction of SRAM cells, a kind of memory. The main problem with long-termmemory is single-eventdisruptions (SEUs), which are brought on by particles ofradiation. Rising urbanization is directly responsible for the SEUs. As CMOS processtechnology has advanced, both the critical charge and supply voltage have decreased.A approach free of these SEUs is needed for use in aircraft systems. Where exactly dothey exist in the very radioactive void between the stars? Methods that are radiation-hardenedby design (RHBD)thatare resistanttosofterrorsarecurrentlybeingresearched.Theprimarycontributionofthisstudyisaproposalforalow-profile,high-reliabilityRHBDmemorycell.

"Adiabaticlogic"referstolow-powerelectricalcircuitsthatmaybeemployedineitherdirection. During the adiabatic phase, there is no change in the total quantity of heat orenergy in thesystem,thusthename.Energy dissipationisgreatlyimprovedbydecreasingcircuitsizeandincreasingcircuitfineness,whichhasbeenamajormotivationforstudyingadiabaticcircuits.

A. SCRLNAND

Understanding the bigpicture behind this group of genes may require dissecting the SCRL NA ND completeloopshowninFigure1.

ThisNDusestrapezoidalclocks(Kin1 and/Kin1)to powerthetopandbottomtracks,rather than the more conventional Vdd and Gne 1. There has been no change to thissection. With the exception of P 1, which is connected to Gnd, and /P 1, which isconnected to Vdd, all components are linked to Vdd/2 in the first position, renderingthe switch gate superfluous. The transmission gate is turned on once P 1 and P 1 areconfigured.Firststeps.VddandGndarethencreatedfromthe/first1and/first1Vdd/2nodes. At this stage, the NA ND of both a and b go through the same non-adiabaticdoorcalculation.Oncetheoutputisbeingutilizedbythesubsequentgate,thetransmitting gate may be gradually disabled. The input may be adjusted and the nextphase initiated once the sum of phases 0 and 1 reaches Vdd/2 again. Since a deviationfrom Vdd/2 would violate the first criterion, a resistor must be disabled and the railsresettothisvalue.

P-MOS'sfunctionwhencoupledwithBinputisunclear.Pleasereviewthecircumstancesbehind thedisappearance ofthe transistor.Timesoftheeleventhday.

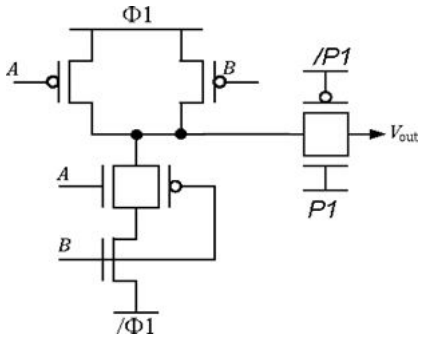

Figure 1 :SCRLNAND

B. 2LAL

Frank's[2] Another significant class of adiabatic circuits is the 2LAL family. Thisseries, like SCRL, has complete plumbing all the way to the gate. Figure 2(a) depictsthe fundamental components of 2LAL, a pair of transmission gates used to representthesignalsAandA.BecauseofitssimplicityandindependencefromCMOS,2LALiswellsuitedforimplementationincutting-edge devices.

Two transmission gates make up the 2LAL basic buffer feature, seen in Figure 2(b).Eachtrapezoidalclock'szero pointonthefourthcyclehappensoneandaquartertimeslater than the other. Both vertices start out with a value of 0 at the beginning. If theinputis1,the state willchangefrom0 to1overtime.Whenwegoonto"phase 1,"

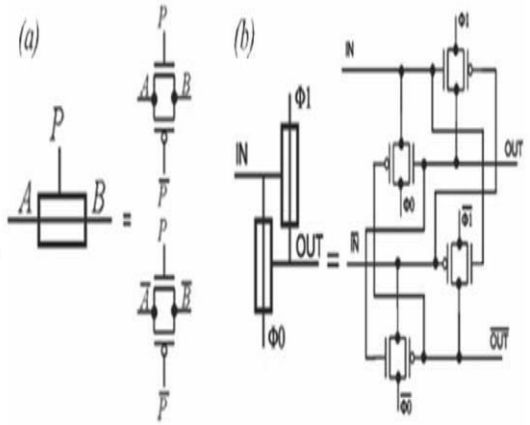

Figure 2: 2LALBasicGate(a) andBuffer(b)

Whentheinput is1,theoutputand inputarebothsetto 1,andthetransistorisdisabledto save power. Finally, switch the input back to 0 and keep cycling between 1 and 0.Thepipelineisreadytoacceptanewinputaftertheoutputpassesthroughthenextgateand reverts to 0. 2LAL can build inverters quickly since rails may cross from one porttoanother.

II. RESULT

A. *Proposed schematic*

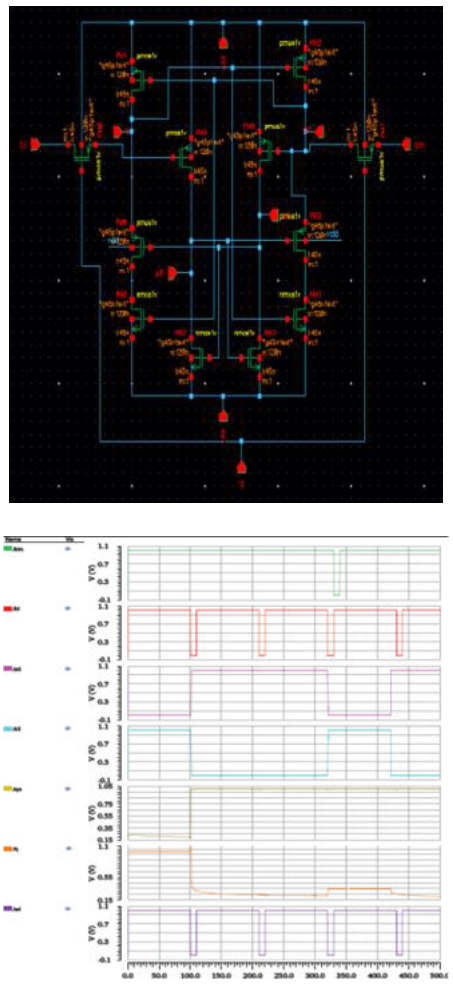

Figure 3: Proposed schematic

Figure 4 : proposed schematic simulation result

A. DELAY

```
Parsing                          0.01 seconds
Setup                            0.05 seconds
DC operating point               0.07 seconds
Transient Analysis               0.03 seconds
Overhead                         0.91 seconds
-----------------------------------------
Total                            1.07 seconds
```

A. POWER

```
Power Results

VVoltageSource_3 from time 0 to 100
Average power consumed -> 5.594084e-011 watts
Max power 2.061770e+000 at time 8.025e-008
Min power 8.198842e-003 at time 3.20774e-008
```

III. CONCLUSION

Soft errors in conventional 65 nm CMOS technology are lessened by the special 12T RHBD memory cell created here. In many ways, the suggested memory cell is better than previous designs, but above all, it is

more resilient to disruptions that harm many nodes. The process's SEU resilience is further supported by 1000 MC simulations, which show that process modifications have no effect on the stability of the SEU. The suggested 12T memory cell's slower read access time in comparison to current memory technologies may slow down some high-speed applications. Mission-critical aviation applications may place a considerably higher value on memory capacity, ruggedness, and dependability. Therefore, compared to other state-of-the-art hardened memory cells, the RHBD 12T memory cell described in this study is a good design for radiation resistance from the perspective of a critical application designer. One typical way to enhance is to speed up the paper while reducing its impact.

The BTI, which alters the transistor's Vth value, is one of the most challenging Nano-scale dependability problems to resolve. SRAM transistors' Vth can be changed to lower the quality of SNMs. In this work, we provide a sensor that can accurately identify BTI degradation in SRAM cells, enabling long-term tracking of this process. The NBTI/PBTI ageing of individual SRAM cells can be approximated by the peak Ivdd/Ignd of the SRAM block during a write operation. This current is measured and converted to voltage by the CCVS. The highest value of this voltage determines the fundamental frequency of the oscillation of the VCO. To see the effect of BTI, the oscillation frequency may be compared to that of freshly generated cells. The BTI state of the row or cell may be revealed by reading the relevant item in the SRAM.

REFERENCES

[1] E. Ibe, H. Taniguchi, Y. Yahagi, K.-I. Shimbo, and T. Toba, “Impact of scaling onneutron-induced soft error in SRAMs from a 250 nm to a 22 nm design rule,” IEEETrans.ElectronDevices,vol.57,no.7,pp.1527–1538,Jul.2010.

[2] P.E.DoddandL.W.Massengill,“Basicmechanismsandmodelingofsingle-eventupset in digital microelectronics,” IEEE Trans. Nucl. Sci., vol. 50, no. 3, pp. 583–602,Jun.2003.

[3] R. C. Baumann, “Soft errors in advanced semiconductor devices part I: The threeradiationsources,”IEEETrans.DeviceMater.Rel.,vol. 1,no.1,pp.17–22,Mar.2001.

[4] H. L. Hughes and J. M. Benedetto, “Radiation effects and hardening of MOStechnology:Devicesandcircuits,”IEEETrans.Nucl.Sci.,vol.50,no.3,pp.500–521,Jun.2003.

[5] C. Boatella, G. Hubert, R. Ecoffet, and S. Duzellier, “ICARE on-board SAC-C:Morethan8yearsofSEUandMCU,analysisandprediction,”IEEETrans.Nucl.Sci.,vol.57,no.4,pp.2000–2009,Aug.2003.

[6] Y.Bentoutou,“ArealtimeEDACsystemforapplicationsonboardearthobservation small satellites,” IEEE Trans. Aerosp. Electron. Syst., vol. 48, no. 1, pp.648–657,Jan.2012.

[7] P. D. Bradley and E. Normand, “Single event upsets in implantable cardioverterdefibrillators,”IEEETrans.Nucl.Sci.,vol.45,no.6,pp.2929–2940,Dec.1998.

[8] M. L. McLain, H. J. Barnaby, I. S. Esqueda, J. Oder, and B. Vermeire, “Reliabilityof high performance standard two-edge and radiation hardened by design enclosedgeometrytransistors,”inProc.IEEEInt.Rel.Phys.Symp.,Apr.2009,pp.174–179.