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Enhanced VLSI Architecture of Partial Product Generator using Redundant Binary Modified Partial Product Generator Method

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ABSTRACT
Adders are fundamental components in arithmetic units, particularly in parallel addition operations that require high speed. Redundant Binary Signed Digit (RBSD) adders are specifically designed for high-speed arithmetic operations. In high-radix Booth encoding algorithms, partial products are minimized during the multiplication process. The Redundant Binary (RB) representation is preferred in designing high-performance multipliers due to its modularity and carry-free addition. Traditional RB multipliers require an extra RB partial product (RBPP) row, necessitated by the error-correcting word (ECW) generated by both the radix-4 Modified Booth encoding (MBE) and the RB encoding. This additional RBPP accumulation stage is required for MBE multipliers. In this paper, we propose a novel RB modified partial product generator (RBMPPG), which eliminates the need for the extra ECW, thereby saving one RBPP accumulation stage. The proposed RBMPPG produces fewer partial product rows than conventional RB MBE multipliers. Simulation results indicate that the proposed RBMPPG significantly reduces area and power consumption, especially when the word length of each operand in the multiplier is 32 bits or more.
Keywords: Redundant Binary, Modified Booth Encoding, RB Partial Product Generator, RB Multiplier.

INTRODUCTION

The advanced multiplier is a critical arithmetic unit in digital circuits, such as in digital signal processors and emerging media processors. It is also a crucial component in application-specific data paths of video and audio codecs, digital filters, computer graphics, and embedded systems. Compared to many other arithmetic operations, multiplication is both time-consuming and power-intensive. In many designs, the critical path is often dominated by the digital multiplier, which may limit the overall speed of the system. Consequently, the design of high-speed multipliers with low energy dissipation remains an active area of research in VLSI design.Redundant Binary (RB) representation is one of the signed-digit representations, first introduced by Avizienis in 1961, for fast parallel arithmetic. Numerous algorithms and models have been proposed to design high-speed, low-power multipliers. A typical binary (NB) multiplication process in digital circuits consists of three stages:

1. Partial Product Generation: Partial products are generated by multiplying the multiplicand by each digit of the multiplier.
2. Partial Product Reduction: The generated partial products are summed using a partial product reduction tree until only two partial product rows remain.
3. Final Addition: The remaining two partial product rows are added using a fast carry-propagation adder.

In the second stage, two methods are commonly used for partial product reduction: using 4-2 compressors or using redundant binary (RB) numbers. Both methods allow the partial product reduction tree to achieve a 2:1 reduction rate. The RB addition is carry-free, making it a promising alternative to two's complement multi-operand addition in a tree-structured multiplier.

Similar to a conventional parallel (NB) multiplier, an RB multiplier is divided into three stages and consists of four modules:

1. Booth Encoder
2. RB Partial Product Generator (RBPPG)
3. RB Partial Product Accumulator
4. RB-to-NB Converter

Radix-4 Booth encoding or Modified Booth Encoding (MBE) is typically used in the partial product generator of parallel multipliers to reduce the number of partial product rows by half. A redundant binary partial product (RBPP) row can be obtained from two neighboring NB partial product rows by inverting one of the rows. An N-bit conventional RB MBE (CRBBE-2) multiplier requires N/4 RBPP rows. Additionally, an error-correcting word (ECW) is required by both the RB and the Booth encoding; hence, the number of RBPP accumulation stages (NRBPPAS) required for a power-of-two word-length (i.e., 2^n-bit) multiplier is given by. This paper focuses on the RBPP generator for designing a 2^n-bit RB multiplier with fewer partial product rows by eliminating the additional ECW. A new RB modified partial product generator based on MBE (RBMPPG-2) is proposed. In the proposed RBMPPG-2, the ECW of each column is shifted to its next neighbor row. Furthermore, the additional ECW generated by the last partial product row is combined with both the two most significant bits (MSBs) of the first partial product row and the two least significant bits (LSBs) of the last partial product row using logic simplification. Thus, the proposed method reduces the number of RBPP rows from \(N/4 + 1\) to \(N/4\), i.e., an RBPP accumulation stage is saved. The proposed technique is applied to 8×8-bit, 16×16-bit, 32×32-bit, and 64×64-bit RB multiplier designs. The designs are synthesized using the NanGate 45nm Open Cell Library. The proposed designs achieve significant reductions in area and power consumption compared to existing multipliers, especially when the word length of each operand is at least 32 bits.

LITERATURE SURVEY

Booth encoding, particularly high-radix Booth encoding strategies, can reduce the number of partial products. However, the number of hard products (i.e., those that cannot be performed by simple shifting and complementation) increases as well. Besli et al. observed that some hard products can be obtained by the differences of two simple power-of-two multiples. A radix-16 Booth encoding technique without ECW has been proposed to avoid the issue of hard products. A radix-16 RB Booth encoder can be used to overcome the hard product issue and avoid the additional ECW, but at the cost of doubling the number of RBPP rows. Consequently, the number of radix-16 RBPP rows is the same as in the radix-4 MBE. However, the RBPP generator based on radix-16 Booth encoding has a complex circuit structure and a lower speed compared to the MBE partial product generator while requiring the same number of partial products.The objective of this study is to implement a modified partial product generator for RB multipliers. An RB multiplier consists of an RB partial product generator, an RBPP reduction tree, and an RB-NB converter. Radix-4 Booth encoding or modified Booth encoding (MBE) is typically used in the partial product generator of parallel multipliers to reduce the number of partial product rows by half. An RBPP row can be obtained from two neighboring NB partial product rows by inverting one of the rows.

Modified Booth Encoder:

To achieve high-speed multiplication, algorithms utilizing parallel counters, such as the modified Booth algorithm, have been proposed. Several multipliers based on these algorithms have been implemented for practical use. This type of multiplier operates significantly faster than a cluster multiplier for longer operands because its computation time is proportional to the logarithm of the operand's word length.Booth multiplication is a technique that enables smaller, faster multiplication circuits by recoding the numbers being multiplied. It is possible to reduce the number of partial products significantly by using the radix-4 Booth recoding technique. The fundamental idea is that instead of shifting and adding for every bit of the multiplier term and multiplying by 1 or 0, we only consider every second bit, multiplying by ±1, ±2, or 0 to achieve the same result.

PROPOSED SYSTEM

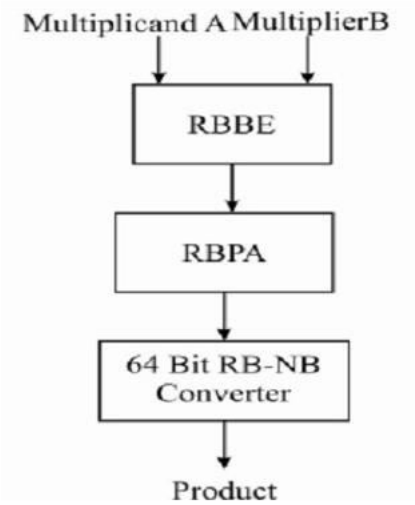


Fig.1 Block Diagram

The advantage of this technique is the halving of the number of partial products. To Booth recode the multiplier term, the bits are considered in blocks of three, such that each block overlaps with the previous block by one bit. The grouping starts from the least significant bit (LSB), and the first block uses only two bits of the multiplier. Figure 3 demonstrates the grouping of bits from the multiplier term for use in the modified Booth encoding.

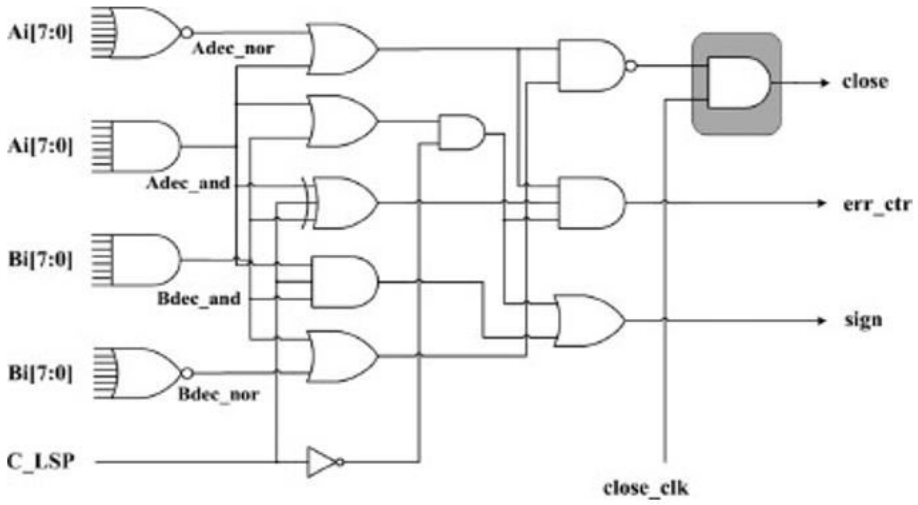


Fig.2 Grouping of bits from the multiplier term

Each block is decoded to generate the correct partial product. The encoding of the multiplier Y, using the modified Booth algorithm, generates the following five signed digits: -2, -1, 0, +1, +2. Each encoded digit in the multiplier performs a specific operation on the multiplicand X, as illustrated in Table 1.For partial

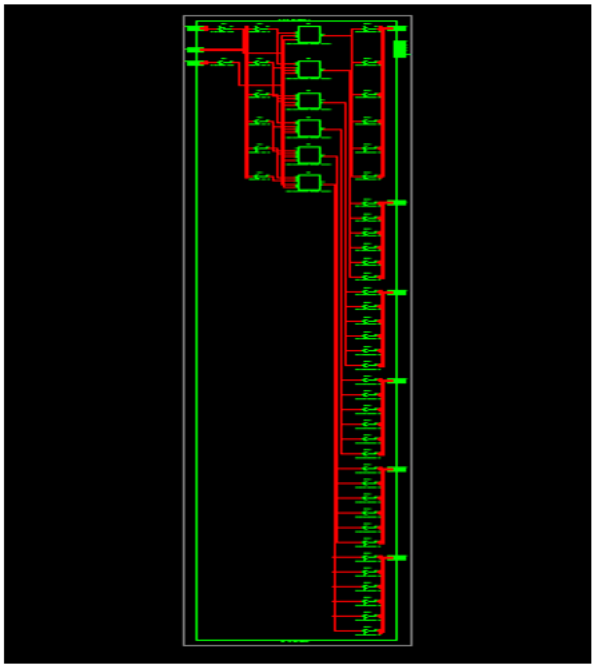
product generation, the radix-4 Modified Booth algorithm is adopted to reduce the number of partial products.

TABLE 1: RB Encoding Scheme

X_i^+	X_i^-	RB digit (X_i)
0	0	0
0	1	$\bar{1}$
1	0	1
1	1	0

Both MBE and RB coding schemes introduce errors, necessitating two correction terms:
1. When the NB number is converted to an RB format, -1 must be added to the LSB of the RB number.
2. When the multiplicand is multiplied by -1 or -2 during Booth encoding, the number is inverted, and +1 mustbe added to the LSB of the partial product.A single ECW can compensate for errors from both the RB encoding and the radix-4 Booth recoding.In this design, we propose a novel RB modified partial product generator (RBMPPG-2) that eliminates the additional ECW introduced by previous designs. As a result, an RBPP accumulation stage is saved due to the elimination of ECW. The new RB partial product generation technique can be applied to any 2n-bit RB multipliers to reduce the number of RBPP rows from \(N/4 + 1\) to \(N/4\). Simulation results have shown that the performance of RBMBE multipliers using the proposed RBMPPG-2 is significantly improved in terms of delay and area. The proposed designs achieve significant reductions in area and power consumption when the word length is at least 32 bits.

Technology Schematic



CONCLUSION

In this paper, we presented a new modified RB partial product generator (RBMPPG-2) that eliminates the additional error-correcting word (ECW) typically introduced by traditional designs. By eliminating this ECW, an entire RB partial product (RBPP) accumulation stage is saved, leading to a reduction in the overall delay, area, and power consumption of the multiplier. This new RB partial product generation technique is applicable to any 2n-bit RB multipliers, reducing the number of RBPP rows. Simulation results demonstrate that the proposed RBMPPG-2 significantly improves the performance of RBMBE multipliers in terms of delay and area. The proposed designs achieve substantial reductions in both area and power consumption, particularly for word lengths of 32 bits or more.

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