

## HIGH-SPEED VLSI ARCHITECTURE FOR EFFICIENT MULTIPLICATION OPERATIONS

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**ABSTRACT:** In a diverse array of digital signal processing scenarios, multipliers are indispensable. Researchers have been diligently striving to develop a multiplier that meets the four criteria of contemporary technology: low power consumption, uniform architecture, small size, and light weight. The study indicates that a four-bit multiplier that is optimized for low power consumption and speed has a variety of prospective applications in the context of very large scale integration (VLSI). An extremely dependable multiplier factor is generated when a mixed single-bit full adder is combined with Dadda mathematical reasoning. It seems that the methodology employed to determine this multiplier was accurate. The recommended multiplier factor reduces energy consumption by 24.5 percent and route delay by 65.9 percent in comparison to the current multipliers. The specter virtuosity app is the most effective stimulant. The EDA program CADENCE 5.1.0 should be employed to ascertain the actual multiplier factor.

**Keywords:** Multiplier; Dadda Algorithm; Gate diffusion Input(GDI);Pass transistor logic(PTL); CMOS process technology; Cadence (tool)

### 1. INTRODUCTION

A multiplier is an important part of computers that work with real-time data. The methods of multiplying and dividing are being improved right now to make them smaller, use less energy, and take less time to run. When used with a half adder and a full adder, the multiplier cuts all numbers by 25% to 35% away. Digital signal processing (DSP) processes on short sequences can be done 40% to 60% faster when high-speed Vedic multipliers are used instead of regular units. Fixed and floating point multipliers were made using a Vedic method, which made digital signal processors more accurate and faster [3]. A lot of different styles and methods have been used to make things more useful and efficient. Dadda, Wallace Tree, Vedic, and Booth all have a lot of pictures in them.

In the next part, we'll talk more about the Dadda algorithm. Part III goes into more detail about the design of the suggested method.

In the fourth part of the paper, the numbers are looked at, and both the suggested and real multipliers are thought about. The story comes to an end with the fifth and final episode.

### 2. DADDA ALGORITHM

It is the goal of the study to speed up the operation of the multiplier by using the Dadda method to shorten the critical path. The suggested multiplier uses a four-bit model to do sixteen different partial multiplications. A 4x4 grid and a 4 leaf tree are used in Figure 1 to show how grid multiplication works. Use the dada method to cut the tree down to just two nodes.

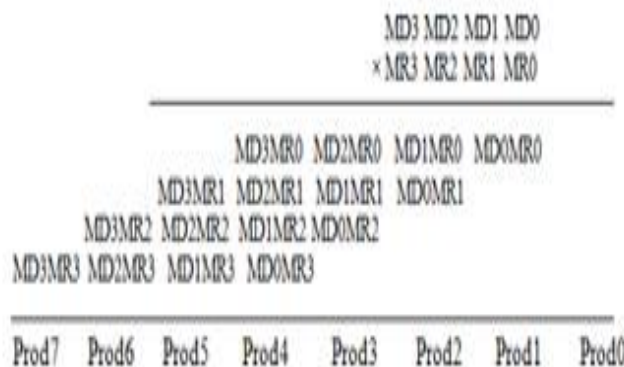


Fig.1.Sample 4x4 Multiplication

The Dadda method shortens the time it takes for information to spread by making it less important to use past level outputs to guess future level outputs. There were only four nodes in the first level of the tree before the dada method was added. At this point, there are only three left. The multiplication tree has three steps up to the second level.



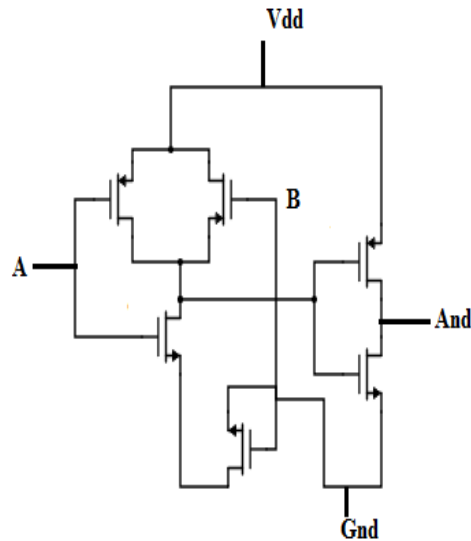


Fig.6.AND Gate

Figure 7 depicts the recommended multiplier for Figure 7 shows the multiplier that should be used in the circuit design of a user with a single adder. The parts can be seen as T1, T2, and T3. Module T1's XOR gate has been changed so that it works with GDI, which stands for Gate Diffusion Logic. Module T2 shows how the PTL's XOR function works, and Module T3 goes into great detail about the MUX function. Taking the results of T1 and T2 and adding them together makes the total adder. When the T3 module is turned on, a carry signal is sent.

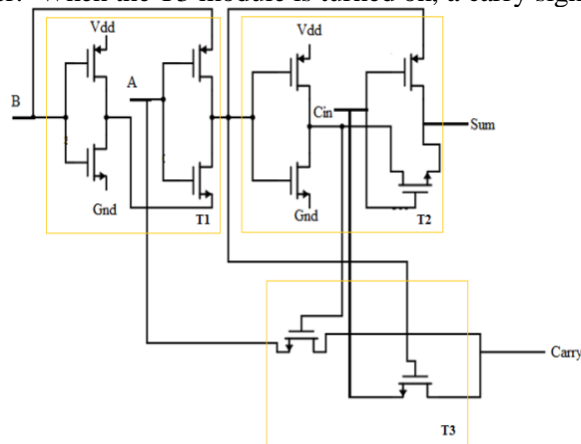


Fig.7.This query depicts a potential architecture for a single-bit full adder.

To add two binary numbers, you need a device with two input lines. This is what you need to make a multiplier. This part is very important for the instrument to work. Four binary adder circuits with two inputs will be needed to build a 4x4 multiplier. Figure 8 shows a CMOS drawing of a binary adder device that can handle two binary numbers. Binary numbers are used to control this gadget.

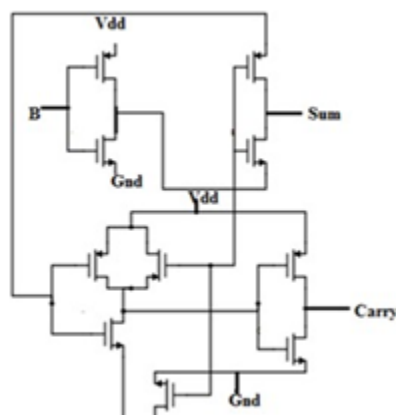


Fig.8.Two input binary digits adder circuit

It is the job of the multiplier to keep the voltage steady and speed up the transfer of data between the first and last steps. Figure 9 shows the information that was given.

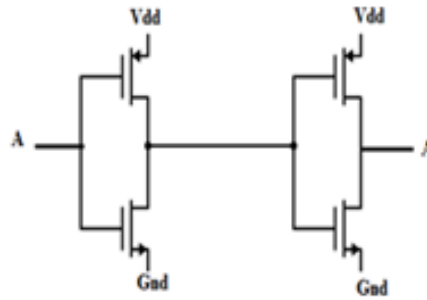


Fig.9.Buffer

#### 4. SIMULATION RESULTS

A machine that can set electrical designs You need to have CADENCE 5.1.0 in order to create factors. Specter Solo can still be used to make it look like different things are happening. Cadence software was used to make the RTL schematic design of the suggested multiplier, which can be seen in Figure 10.

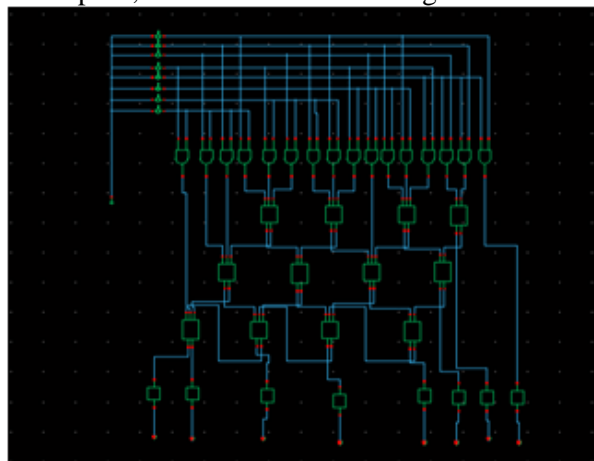


Fig.10.A diagram displaying the technology that was to be employed in the development of the system. The picture above shows how the suggested 4-bit multiplier would react to any changes in the input data. This word "indicates" what will happen with the multiplier, which is made up of Prod0, Prod1, Prod2, Prod3, Prod5, Prod6, and Prod7.

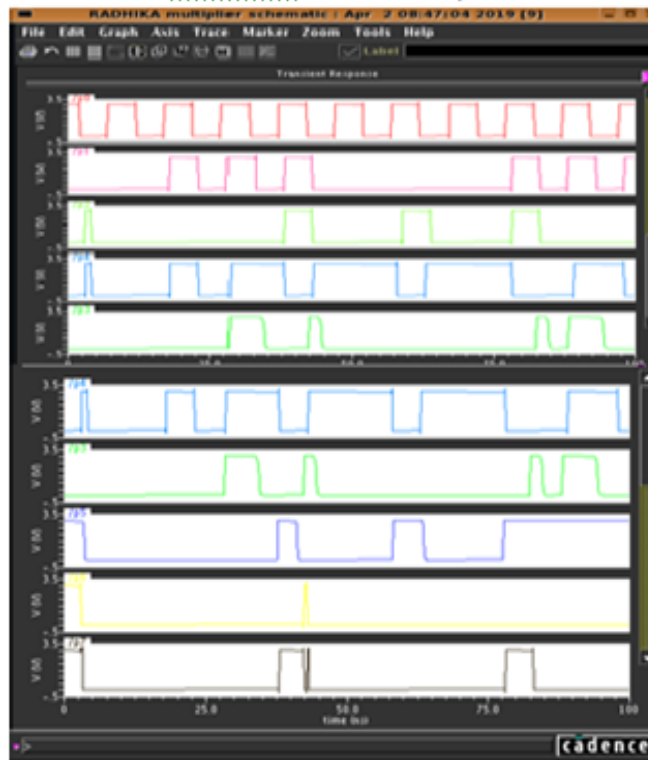


Fig.11. Transient response of the multiplier

The steps for figuring out power and delay in timing are shown below.

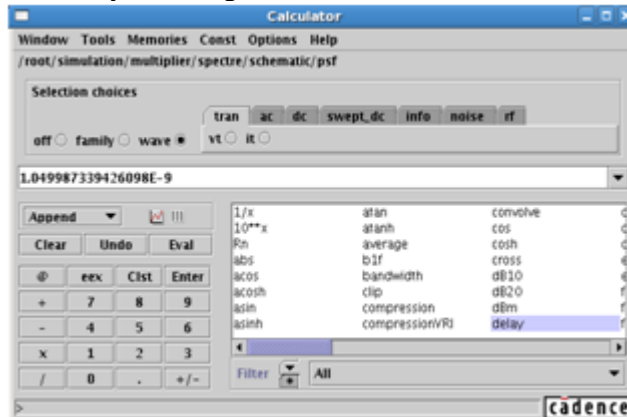


Fig.12. Power calculation in cadence

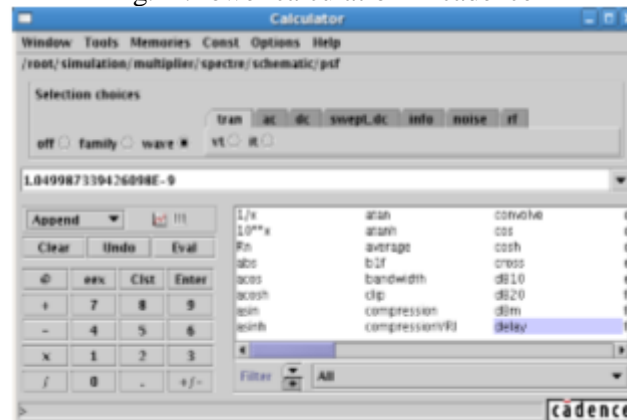


Fig.13. Delay calculation in cadence

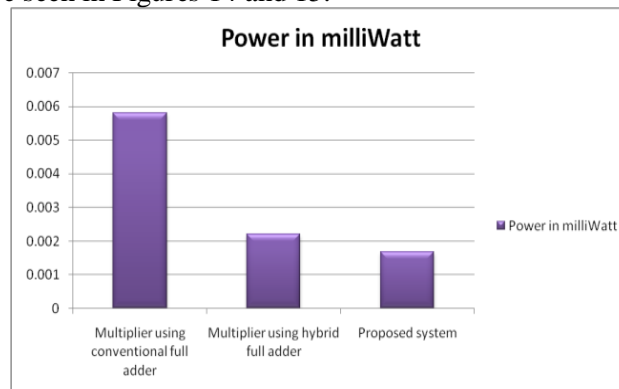
**Table I. Comparison of Different Multipliers**

No	Multiplier	No of transistors	Power in mW	Delay in ns
1	Using Conventional CMOS Full Adder	392	0.0058	3.834
2	Using Hybrid Full Adder (Existing)	264	0.00224	3.0603
3	4-bit Dadda Multiplier using Compressor	376	1.172	0.353
4	DADDA Tree Multiplier Using Adiabatic Logic	-	77	-
5	4-bit Static CMOS based DADDA Multiplier	316	-	-
6	<b>Proposed Multiplier</b>	<b>248</b>	<b>0.00169</b>	<b>1.0409</b>

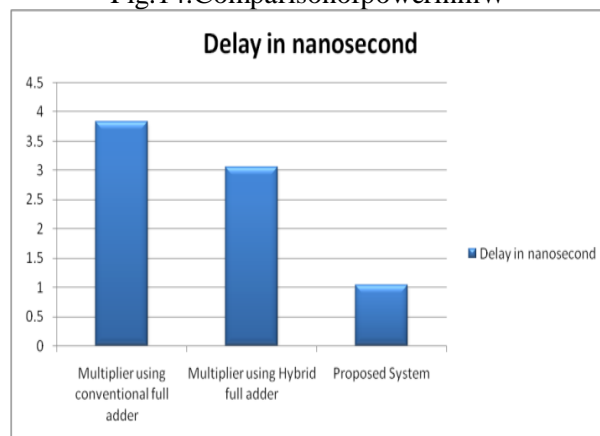
Table I shows the effectiveness rates of multipliers that use full adders. This includes the number of transistors, the amount of power used, and the length of the critical path. The multiplier that was suggested makes the circuit easier to understand, uses less power (1.69W), and shortens the critical path.

The CPU speed and timing delay are shown in the table below. One of the suggested multipliers has a latency of 1.04 ns, which is a lot less than the other multipliers.

The power and delay plots can be seen in Figures 14 and 15.



**Fig. 14. Comparison of power in mW**



**Fig. 15. Comparison of delay in nanosecond**

For example, Table II shows how the different parts of a 4-bit multiplier are used in terms of reasoning.

**Table II. Logic Utilization of Various Modules**

Module	No of transistors	Technique used
Full adder(area and power efficient single bit full adder)	80	Sum: GDI XOR Carry: PTL XOR
Half adder	40	CMOS Processtechnology
Buffer	32	CMOS Processtechnology
AND gate	96	CMOS Processtechnology

## 5. CONCLUSION

A hybrid gadget was used to build the 4-bit multiplier. It can add two binary numbers together thanks to its one-bit adder and three inputs. There are no problems with the circuit. The goals of this design are to make the circuit more complicated while using less power and creating less response time. Because they use little power and spread quickly, PTL and GDI adder circuits work well with three binary numbers. Together, these two changes make the circuit work better as a whole. To get the fastest data flow and response time, a hybrid three-input binary-digit adder circuit is used. Dada is used to cut down on communication delays. A multiplier with a factor of 44 and a delay of only 1.04 ns was shown to work. It is thought to use about 1.69 watts of power on average. Most likely, the size will be smaller than that of a normal repeat.

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