# Optimization of Diode-Clamped Multilevel Inverter by Using Switching Losses and THD

**Maramreddy Harsha Vardhan Reddy**[1]
[1]*Associate Professor, E.E.E Department, GPREC, Kurnool, AP, India.*
*maramreddyharsha@gmail.com*

**Gudipati Kishor**[2]**,**
[2]*Associate Professor, E.E.E Department, GPREC, Kurnool, AP, India.*
*gudipatikishor@gmail.com*

**Repalle Rohit**[3]
[3]*Research Scholar of JNTUA, GPREC Research Centre, AP, India.*
*repallerohit@gmail.com*

***Abstract:*** **-** Square wave or quasi-square wave voltage may be suitable for low- and medium-power applications, but sinusoidal waveforms with minimum distortion are necessary for high-power applications. Harmonic content in the output of a dc–ac inverter can be reduced using either a filter circuit or pulse width modulation (PWM) techniques. Filters have the problem of being huge and expensive, whereas PWM approaches reduce or eliminate the need for filters, depending on the type of application. Traditional two-level pulse width modulation inverters produce less distorted current and voltage at the expense of larger switching losses due to high switching frequency. Traditional two-level high-frequency PWM inverters have a number of disadvantages, including the generation of common-mode voltages, higher switching losses, the need for switches with very short turn-on and turn-off times, a large dv/dt rating, the issue of voltage sharing in series connected devices, and the introduction of a large number of higher order harmonics. To overcome the mentioned issues, multilevel inverters have developed better equivalents to the traditional two-level pulse width modulated inverters. They also have a lower harmonic content at low switching frequencies, resulting in less switching stress on each device for high voltage, high power applications. On the basis of THDs and switching losses at various switching frequencies, this study explores two-level inverters, three-level & five-level diode clamped three-phase inverters. An comprehensive simulation study was conducted to optimize the switching frequency based on the corresponding switching losses and THD contents in line voltage have been presented in this thesis. A sinusoidal pulse width modulation (SPWM) technique is used for control.

***Keywords —total harmonic distortion, multilevel inverter, and switching frequency***

## I INTRODUCTION

Power electronic converters are widely employed in both utility and driving applications in industrial power conversion systems. To achieve satisfactory efficiency, the voltage is increased in proportion to the increase in power.A multilevel converter can be implemented in a variety of methods, each with its own set of benefits and drawbacks. To create multilayer waveforms, the simplest ways include connecting standard converters in parallel or series. Convertors are efficiently inserted within converters in more sophisticated structures. Whatever strategy is adopted, the multilayer converter's future voltage or current rating becomes a multiple of the individual switches, allowing the converter's power rating to exceed the limit required by the individual switching devices.

## II PWM TECHNIQUES FOR MULTILEVEL INVERTERS

### *A.Introduction:*

Multilevel inverters are the most important in terms of harmonic content reduction [10, 12]. They're especially good for high-power situations where semiconductor devices can't operate at high switching frequencies. It's also worth mentioning that when



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solid-state switches are used, the greatest potential switching frequencies are reduced even more. The multilayer structures allow for a very natural and forceful increase in the power handled in the conversion operations..
It is apparent that by using more than two voltage levels to create a sinusoidal form, we can reduce the current harmonics in the load. The actual improvement of the current spectrum, however, is dependent on the control strategy used.

**Principle of PWM Technique:**
Figure 1 shows a schematic diagram of a single-phase inverter with a center-tapped grounded DC bus, and Figure 2 shows the principle of pulse width modulation..

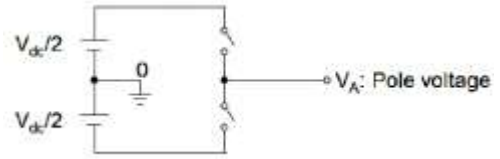



Fig. 1 Circuit Model of Three -Phase Inverter

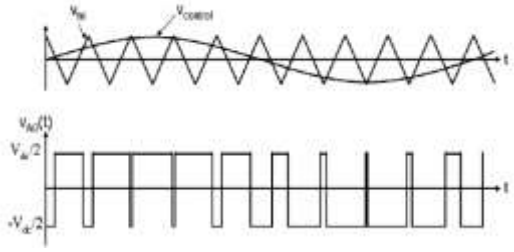
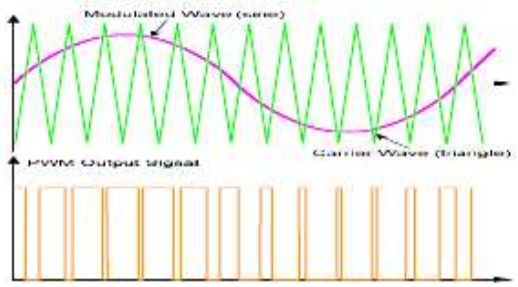


Fig.2 Pulse Width Modulation

As depicted in Fig.2, the inverter output voltage is determined in the following:
When $V_{control} > V_{tri}$, $V_{A0} = V_{dc}/2$
When $V_{control} < V_{tri}$, $V_{A0} = -V_{dc}/2$
Also, the inverter output voltage has the following features:
The peak value of Vcontrol controls the amplitude of PWM, which is the same as the frequency of Vtri.
The frequency of Vcontrol controls the fundamental frequency.
Modulation index (m) is defined as
$m=V_{control} / V_{tri}$
*B. Basic Principle OF SPWM*
In the power inverter and motor control fields, SPWM is one of the most prevalent and successful PWM systems. The sine-triangle wave analogy is a useful method to explain its main features. When the triangle wave's instantaneous value is less than the sine wave's, the PWM output signal is high (1). Otherwise, it will be demoted to the bottom tier (0). The level switching edge is generated whenever the sine wave touches the triangle wave. The duty cycle of the output waveform fluctuates as a result of the various crossing points.




*D.Switching Losses calculation:*



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When a switch is turned on, the current that passes through it is known as idc. To make the calculations easier to understand, the switching waveforms are represented using linear approximations. Switching losses can be calculated using the devices' turn-on and turn-off characteristics. The instantaneous voltage and current are measured during the turn-on period tc(on).

$v(t)=V_{dc}-(V_{dc}-V_{on})*(t/t_{c(on)});0<t\leq t_{c(on)}$ ----------(1)

$i(t)=I_{dc}*(t/t_{c(on)});0<t\leq t_{c(on}$ --------(2)

Instantaneous power during the interval $t_{c(on)}$ is

$p(t) = v(t)*i(t)$

$=\{V_{dc} - (V_{dc} - V_{on})*(t/t_{c(on)})\}* \{I_{dc} * (t/ t_{c(on)})\}$

$=\{V_{dc} *I_{dc} * (t/ t_{c(on)}) \} - (V_{dc} - V_{on})*(t_2/t_{c(on)} )\}$ …(3)

And energy dissipated during this interval is $t_{c(on),}$

$E_{c,\ on} = \int[\{V_{dc}*I_{dc}*(t/ t_{c(on)})\}- (V_{dc} - V_{on})* )*(t_2/t_{c(on)}^2)]$ dt 0 to $t_{c(on)}$ …(4.4)

$E_{c,\ on} = (V_{dc} *I_{dc} * t_{c(on)})/2 - (V_{dc} - V_{on})* I_{dc} * t_{c(on)}/3$

$=(V_{dc}*I_{dc}*t_{c(on)})/6-(V_{on}*I_{dc}*t_{c(on)})/3$ …(4)

and during turn-off transition, of $t_{c(off),}$ the current falls from $I_{dc}$ to zero and the $V_{on}$ rises linearly to $V_{dc}$.

The instantaneous voltage and current during this period are

$v(t)=V_{on}+(V_{dc}-V_{on})/t_{c(off)}$ …(5)

$i(t)=I_{dc}-I_{dc}/t_{c(off)}$

The instantaneous power dissipated during the interval

$p(t) = v(t)*i(t)$

$= \{V_{on} + (V_{dc} - V_{on})*(t/t_{c(off)})\}* \{ I_{odc} - I_{dc} * (t/ t_{c(off)})\}$

$= V_{on}*I_{dc} + (V_{dc}-V_{on})*I_{dc}*(t/t_{c(off)}) - V_{on}*I_{dc}*(t/t_{c(off)}) -(V_{dc} - V_{on})*I_{dc}*(t_2/t_{c(off)}^2)$ … (6)

Hence, the energy dissipated can be found as $t_{c(off),}t_{c(off)}$ is

$E_{c,\ off} = \int[ V_{on}*I_{dc} + (V_{dc} - V_{on})*I_{dc}*(t/t_{c(off)}) - V_{on}*I_{dc}$

$*(t/t_{c(off)})-(V_{dc} - V_{on})*I_{dc}*(t_2/t_{c(off)2})]$ dt 0 to $t_{c(on)}$

$=(V_{dc}*I_{dc}*t_{c(off))/}6)-(V_{on}*I_{dc}*t_{c(off))/}3)$ … (7)

With a switching frequency of Fs, the average switching loss in the switch during each transition of turn on and Turn off can be found as

$P_{c,\ on} = \{(V_{dc}*I_{dc}*t_{c(on)}/T_s)/6\}+\{(V_{on}*I_{dc}*t_{c(on)/}T_s)/3\}$ …(8)

$P_{c,off}= \{(V_{dc}*I_{dc}*t_{c(off)/}T_s)/6\}-\{(V_{on}*I_{dc}*t_{c(off)/}Ts)/3\}$ -----(9)

Hence, the average switching loss $P_{sw}$ in the switch is

$P_{sw}=(1/6)*V_{dc}*I_{dc}*\{t_{c(on)+}t_{c(off)}\}/T_s +\{(1/3)*V_{on}*I_{dc}*\{t_{c(on)} + t_{c(off)\}/}T_s \}$ …(10)

## III ANALYSIS OF TWO LEVEL DIODE CLAMPED INVERTER

### A Introduction:

The basic circuit of a two-level diode clamped multi-level inverter is discussed in this chapter. For various carrier frequencies, switching losses and total harmonic distortion calculations are performed.

### B Inverter with two levels of diode clamping:

In numerous low-medium-power applications, this is the most often utilised topology. Figure 3 shows the full-bridge layout of the three-phase voltage source inverter. Table 1 shows the switching logic for obtaining output voltage in a 1200 mode of operation. Using PWM techniques, this design can be employed at a very high switching frequency to achieve reduced THD.



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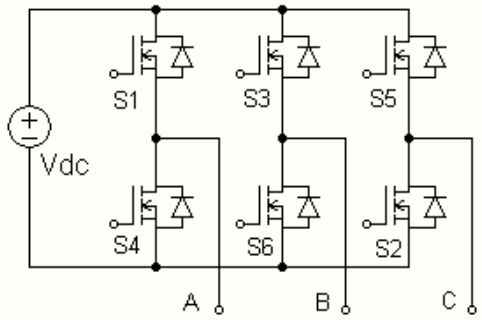


Fig 3 Three phase two level diode clamped inverter

Two switches in a two-level inverter operate simultaneously in the following order: S1 S6, S1 S2,S2 S3,S3 S4,S4 S5,S5 S6. Between the turning on and off of two switches on each leg, there is a 600-second delay. As a result, the short circuit is avoided. In this conducton arrangement, one load terminal remains floating because only two switches are active at the same time. According to the time of switch conduction, a 2-level inverter is classed as 1800/1200 conduction modes. Table 1 lists the switch combinations that can be used to create two level voltages.

Table 1 switching states of two level inverter

| Load line voltage($v_{ab}$) | Switching states | | | | | |
|---|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ |
| $+v_{dc}/2$ | 1 | 0 | 0 | 0 | 0 | 1 |
| $+v_{dc}/2$ | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| $-v_{dc}/2$ | 0 | 0 | 1 | 1 | 0 | 0 |
| $-v_{dc}/2$ | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |

**IV ANALYSIS OF THREE LEVEL DIODE CLAMPED INVERTER**

A Introduction:

The basic circuit of a three-level diode clamped multi-level inverter is discussed in this chapter. For different carrier frequencies, switching losses and total harmonic distortion are calculated..

B Three Level Diode Clamped inverter:

Figure 4 depicts the internal structure of a three-level diode-clamped frequency inverter. (An inverter with a neutral-point clamped frequency is also known as a frequency inverter with a neutral-point clamped frequency.) Two series-connected capacitors C1 and C2 separate the DC-link voltage into three levels. The diodes D1 and D1' are the most significant distinction between three- and two-level inverters. The switching voltage is limited to half the DC-link voltage by these two diodes.



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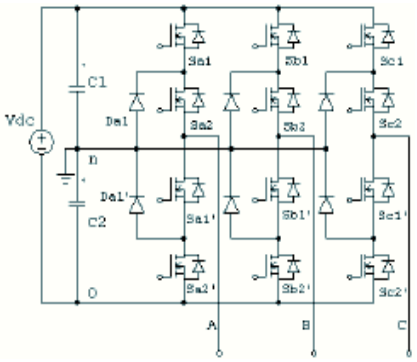


Fig 4 Three level diode clamped inverter

A three-level inverter can give three different output voltage levels $V_{DC}/2$, 0, and $-V_{DC}/2$.

Table 2 switching states of three level inverter

| Sa 1 | Sa2 | S' a1 | S'a2 | Switching states | Output Voltage(VA 0) | Output Phase Voltage(VAn) |
|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | + | $+V_{dc}$ | $+V_{dc}/2$ |
| 0 | 1 | 1 | 0 | 0 | $+V_{dc}/2$ | 0 |
| 0 | 0 | 1 | 1 | - | 0 | $-V_{dc}/2$ |

The steps to synthesize the three level voltages ($+v_{dc}$, $-v_{dc}$ and 0) as follows:

- For voltage level VDC/2 switches S1 and S2 need to be turned on.
- For voltage level -VDC/2 switches S1' and S2' need to be turned on.
- For voltage level 0 switches S1 and S1' or switches S2 and S2' need to be turned on.

To obtain the desired voltage levels, the switching devices in all legs must operate in the same order. The switches are set up to work in accordance with the 1200 phase shift between the three leg voltages. The principle is explained in Table 2.

## V ANALYSIS AND SIMULATION OF FIVE LEVEL DIODE CLAMPED INVERTER

### A Introduction:

The basic circuit of a five-level diode clamped multi-level inverter is discussed in this chapter. For various carrier frequencies, switching losses and total harmonic distortion calculations are performed.

B Five level diode clamped inverter:

Figure 5 shows a four-capacitor dc bus with a single-phase full bridge five-level diode-clamp converter (C1,C2,C3, and C4). The voltage stress across each device is Vdc/4 due to the Vdc/4 voltage across each capacitor..

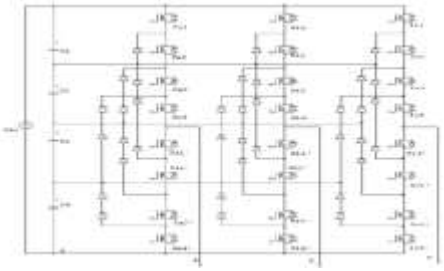

**Fig 5 Five level diode clamped inverter**

The negative dc rail, 0, is used as the output phase voltage reference point to show how the staircase voltage is synthesised. There are five switch combinations in the 5-level converter depicted in Fig 5 to create five level voltages across a and 0.For voltage level $V_{a0} = V_{dc}$, turn on all upper switches Sal through Sa4.



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- For voltage level $V_{ao} = 3V_{dc}/4$, turn on three upper switches Sa2 through Sa4 and one lower switch Sa'1.
- For voltage level $V_{a0} = V_{dc}/2$, turn on two uppers witches Sa3 and Sa4 and two lower switches Sa'l and Sa'2**.**
- For voltage level $V_{a0} = V_{dc}/4$, turn on one upper switch Sa4 and three lower switches Sa'1 throughSa'3.
- For voltage level $V_{a0} = 0$, turn on all lower half switches Sa'1 through Sa'4.

**Table 3 Switching states of five level inverter**

| Output $V_{a0}$ | Switching states | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | $S_{a1}$ | $S_{a2}$ | $S_{a3}$ | $S_{a4}$ | $S_{a'1}$ | $S_{a'2}$ | $S_{a'3}$ | $S_{a'4}$ |
| $V_5=V_{dc}$ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| $V_4=3V_{dc}/4$ | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| $V_3=V_{dc}/2$ | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| $V_2=V_{dc}/4$ | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| $V_1=0$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

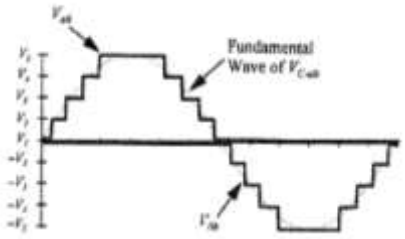


Fig 6 phase and line voltages of 5-level inverter

## VI RESULTS AND DISCUSSION

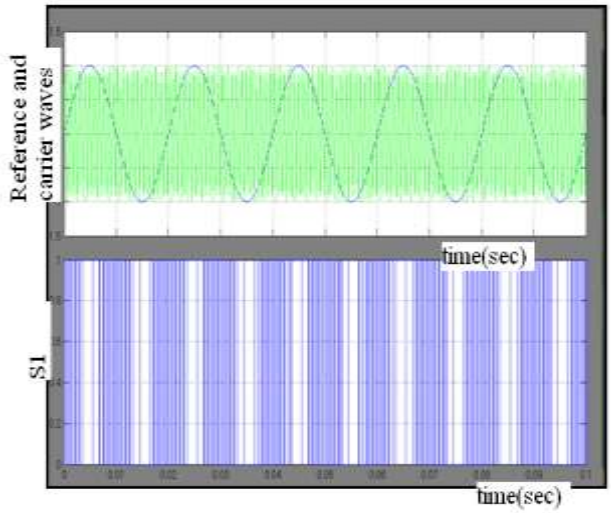


Fig 7 Pulse Generation Waveforms



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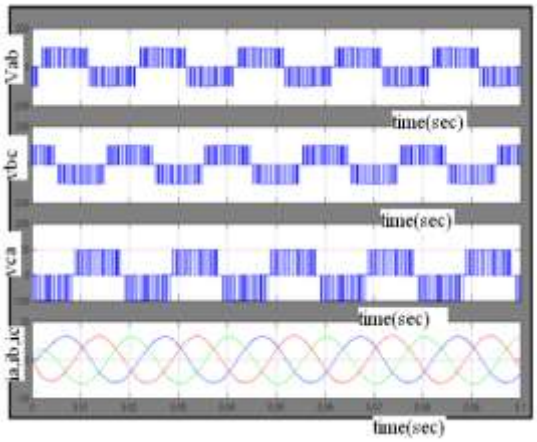


Fig 8.Voltage and Current Waveforms

The generation of switching pulses for the two-level inverter's power device S1 is shown in Fig 8. To generate switching pulses, a triangular carrier wave is compared to a sinusoidal reference wave. The complementary of this pulse is to be given to power device S4.

Table 4 THD and Switching losses for a two-level inverter at different switching frequencies

| Carrier frequency(HZ) | %THD | | | Total switching losses(mj) |
|---|---|---|---|---|
| | Phase A | Phase B | Phase C | |
| 1500 | 44.26 | 44.35 | 44.82 | 25.80 |
| 2500 | 40.48 | 40.73 | 40.63 | 47.68 |
| 3500 | 37.56 | 37.42 | 37.61 | 62.35 |
| 5000 | 31.83 | 31.54 | 31.67 | 88.18 |

THD and switching losses in each phase voltage at various switching frequencies are shown in Table 4. THD decreases as the switching frequency is raised. The frequency ranges between 1500 and 5000 hertz.

Table 4 shows that when the carrier frequency decreases, the switching losses decrease. This is because there are fewer "sampling points" at lower carrier frequencies, which limits the number of switching transitions in a single PWM switching cycle, resulting in lower switching losses.

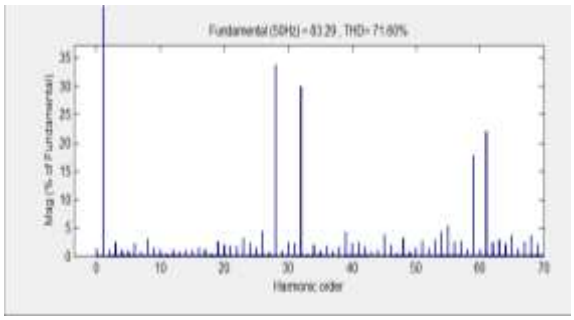


Fig 9 Two level inverter frequency spectrum analysis



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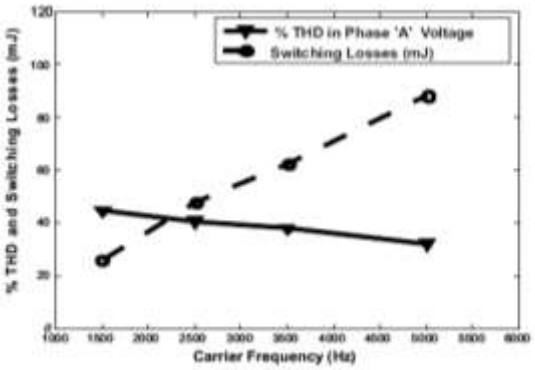


Fig 10 Variation of switching losses and THD with carrier frequency for the two-level inverter

A graph of THD and switching losses with regard to carrier frequencies is produced from the values of THD and switching losses obtained to determine the optimal point with the least amount of losses, as illustrated in Figure 10.

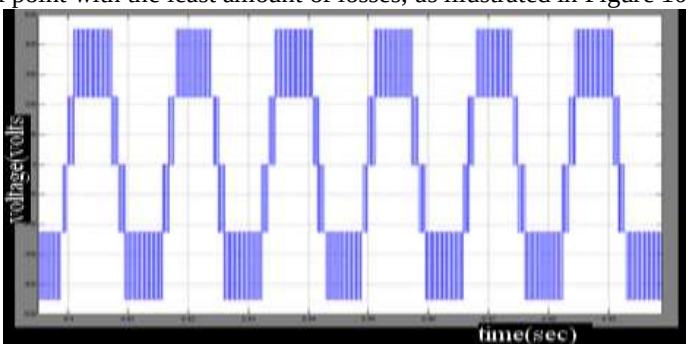


Fig 11.Three level inverter output Voltage waveform

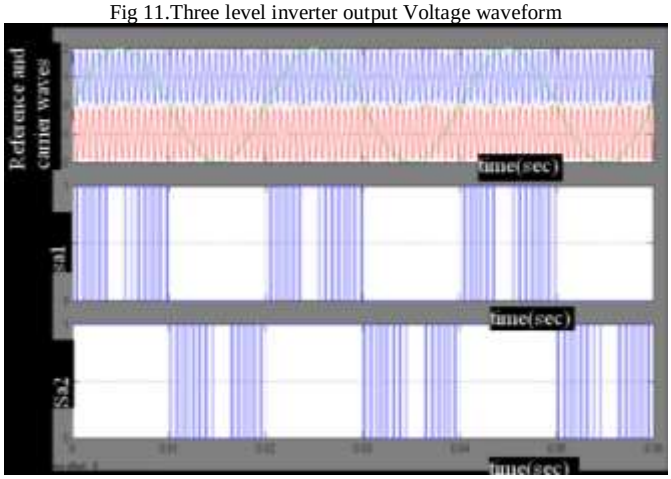


Fig 12 pulse generation waveforms

Figure 12 depicts the generation of switching pulses for the three-level inverter's power devices Sa1 and Sa2. These pulses are complimentary to the pulses for the lowest two devices, Sa1' and Sa2'. THD and total switching losses for several carrier frequencies spanning from 1500 to 5000 HZ are estimated and summarised in Table 4.2. According to the simulation and analysis results for the three-level three-phase inverter, the system performance improves as the number of levels increases in terms of THD and switching losses. In comparison to a two-level inverter, the voltage impressed over the terminals of the switches is



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lowered from 200 to 100 volts. However, it is also noted that for the three-level inverter, an unequal device rating would be required..

**Table 5 THD and Switching losses for a three-level inverter at different switching frequencies**

| Carrier frequency(HZ) | %THD | | | Total switching losses(mj) |
|---|---|---|---|---|
| | Phase A | Phase B | Phase C | |
| 1500 | 34.10 | 34.13 | 33.94 | 21.88 |
| 2500 | 22.05 | 22.39 | 22.52 | 31.86 |
| 3500 | 14.68 | 14.93 | 14.89 | 39.40 |
| 5000 | 8.97 | 8.64 | 9.16 | 46.64 |

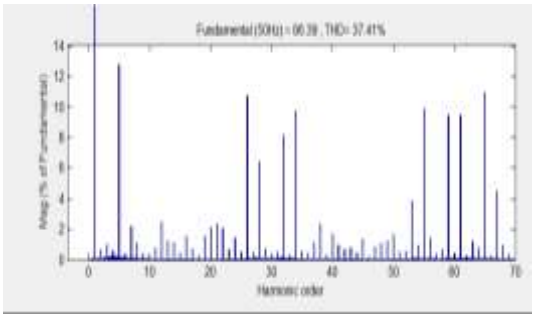

Fig 13 Three level inverter frequency spectrum analysis

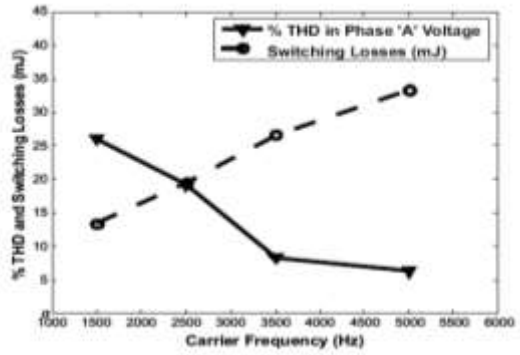


Fig 14 Variation of switching losses and THD with carrier frequency for the three-level inverter

Table 5 shows that lowering the switching frequency from 5000 to 1500 Hz reduced switching losses by nearly half. However, this comes at the cost of a higher THD level. The switching loss and THD levels associated with various carrier frequencies were recorded, and a graph of THD and switching loss fluctuation with carrier frequency was generated to determine the optimum point, as shown in Figure 14.



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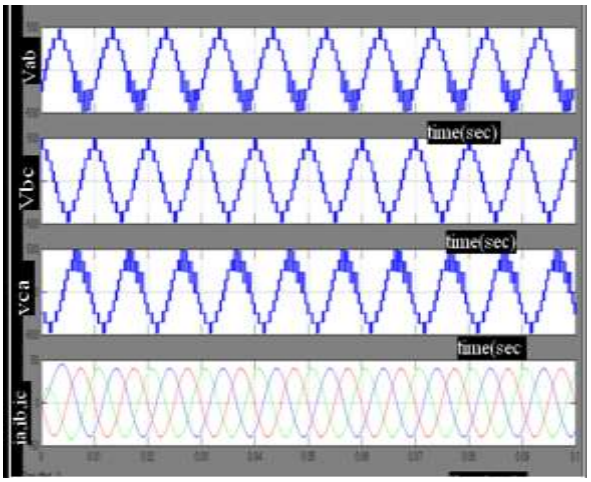


Fig 15 Output voltage and current waveforms

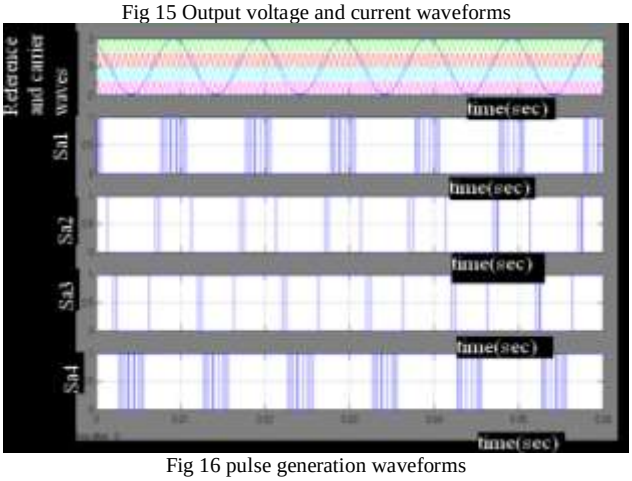


Fig 16 pulse generation waveforms

The generation of switching pulses for the fivelevel inverter's power devices Sa1, Sa2, Sa3, and Sa4 is shown in Fig 16. These pulses are complimentary to the pulses for the lower four devices, Sa1', Sa2', Sa3', and Sa4. Vt1, Vt2, Vt3, Vt4 are the four carrier signals, while Vr is the reference sin wave.

Table 6 THD and Switching losses for a five-level inverter at different switching frequencies

| Carrier frequency(HZ) | %THD | | | Total switching losses(mJ) |
|---|---|---|---|---|
| | Phase A | Phase B | Phase C | |
| 1500 | 18.80 | 18.79 | 18.86 | 13.33 |
| 2500 | 18.24 | 18.20 | 18.23 | 19.84 |
| 3500 | 17.77 | 18.03 | 17.77 | 26.23 |
| 5000 | 17.70 | 17.78 | 17.70 | 35.54 |



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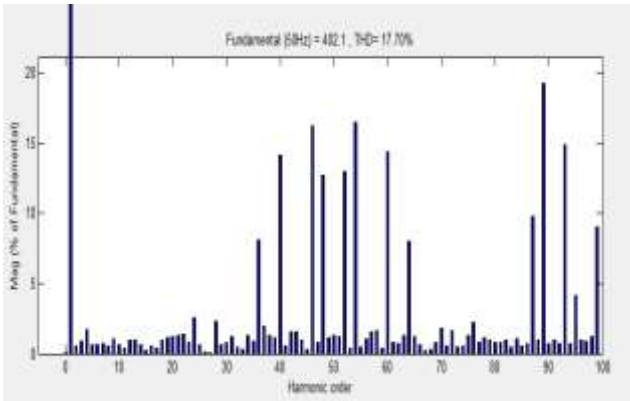


Fig 17 Frequency spectrum analysis

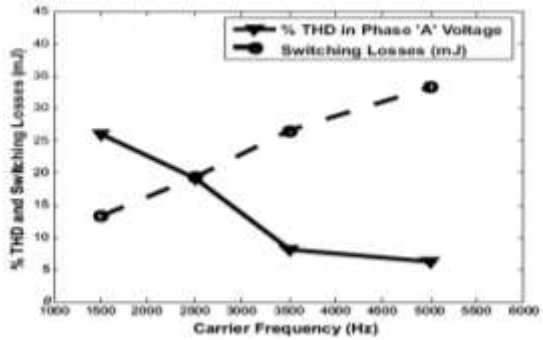


Fig 18 Variation of switching losses and THD with carrier frequency for the five-level inverter

The switching losses and harmonic contents for operation of an inverter at an optimal switching frequency are shown in Fig18. The research described above was conducted without the use of an output filter. The harmonic content can be further lowered by employing appropriate filters..

**VII CONCLUSION**

This paper utilizes the SPWM technique to compare the THD of the output voltage waveform and switching losses of two-level, three-level, and five-level three-phase diode clamped inverters. With an increase in the number of levels in the Output voltage, both THD and switching losses are shown to decrease. However, as the carrier frequency is reduced, the THD level rises and switching losses fall accordingly..

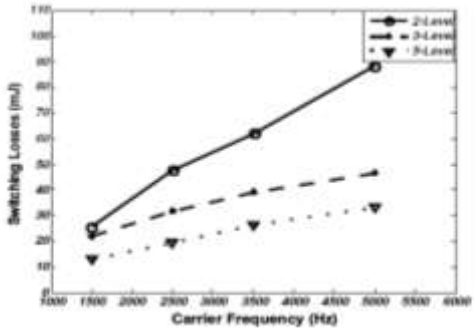


Fig 19 Variation of switching losses for two level, three level and five-level inverters with carrier frequency



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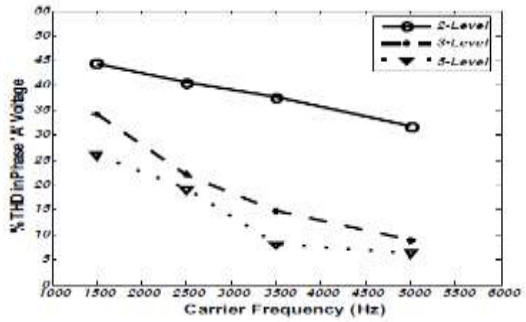


Fig 20 Variation of %THD for two level, three level and five-level inverters with carrier frequency

Switching losses and THD for two-level, three-level, and five-level inverters are shown in Figures 19 and 20, respectively. At a given switching frequency, switching losses are shown to decrease as the number of levels in the output voltage increases. Switching losses rise with switching frequency for the same inverter level. THD decreases with the number of inverter levels and switching frequency, as seen in Figure 20.

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