

HIGH-SPEED, LOW-POWER FULL ADDER DESIGN USING MUX IN 16NM CMOS TECHNOLOGY

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Abstract-

This project proposes new circuits for simultaneous XOR–XNOR and XOR/XNOR operations. The low output capacitance and low short-circuit power dissipation of the suggested circuits result in highly optimised power usage and delay. Additionally, we suggest six brand-new hybrid 1-bit full-adder (FA) circuits that are built on the innovative full-swing XOR–XNOR or XOR/XNOR gates. Regarding speed, power consumption, power delay product (PDP), driving capability, and other factors, each of the suggested circuits has advantages of its own. Comprehensive HSPICE and Cadence Virtuoso simulations are run to examine the performance of the suggested designs. The suggested solutions outperform previous FA designs in terms of speed and power, according to the simulation findings, which are based on Tanner's 16-nm CMOS process technology model. A novel approach of transistor sizing is used in order to maximise the circuits' PDP. The suggested approach uses the particle swarm optimisation technique for numerical computing to reach the target value for the optimal PDP with fewer iterations. Variations in the supply and threshold voltages, output capacitance, input noise immunity, and transistor size are examined in the suggested designs.

Key words: HSPICE, swarm optimization

I. INTRODUCTION

In the modern world, electronic systems are essential to daily existence. Electronic systems include digital gadgets like signal processors, microprocessors, and communication devices. The use of circuits [1] is limited to low power and space consumption as the need for electronic systems rises. As a result, the demand for portable devices like laptops, tablets, and cell phones has grown significantly due to population and technological growth. To meet this demand, designers have created circuits that use less energy and space while increasing speed. Adder circuits, multiplier circuits, and divider schematics are examples of digital applications that are efficient in performing arithmetic operations. The chip density for circuit design is growing as technology advances. Consequently, a large number of transistors are doped into a single chip.

II. EXISTING METHOD

The Existing method XOR–XNOR circuit is saving almost 16.2%–85.8% in PDP, and it is 9%–83.2% faster than the other circuits. The circuits of Fig. 1(d) and (e) have the very high delay due to its output feedback (which have the slow response problem). As can be seen in Table I, the efficiency of Fig. 1(e) is much worse and its delay is four times more than that of other circuits. Table I indicates that the structures have shown a better performance, which have the minimum NOT gates on the critical path and also have not feedback on the outputs to correct the output voltage level. To better evaluate the XOR–XNOR circuits, they are simulated at different power supply voltages from 0.6 to 1.5 V and also at different output loads from FO1 to FO16. The results of these two simulations are shown in Fig. 5(b) and (c). As seen in Fig. 5(b) and (c), the proposed XOR–XNOR circuit has the best performance in both simulations when compared with other structures.

The two input signal A, B are given to transistors. The signal B is given to P2 and signal A is given to P3. The signal B is given to N2 and P4 and the signal A is given to N2 and N3. The N3 is connected to P4. The signal B is given to N4 and P6 and the signal A is given to P5 and P6.

The N4 is connected to N5. The signal B is given to N5 and the signal A is given to N6. The transistors P4

and N4 are shorted together and the out is Abar. The signal A is given to N9 and Ci is given to P9. The N2 and N3 transistors are shorted together and output is given N7 and Ci is given to N7, Ci is given to P7. The N2 and N3 transistors are shorted together and output is given N7 and N8. The P5 and P6 transistors are shorted together and output is given P7 and P8. Ci is given to N8, P8. The output to N2 and N3 is given to N9 and P9 and output of P5 and P6 is given to N10 and P10. The signal Ci and B is given to N10 and P10. The output of N7 and P7 and output of N8 and P8 are shorted together and the output is sum. The output of N9, P9 and N10, P10 are shorted together and output is carry. The circuit is simulated in 65nm technology and result are obtained.

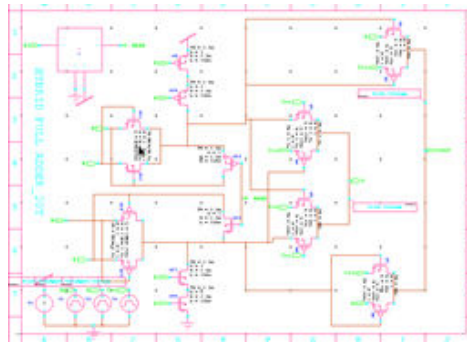


Figure 1: Schematic Of Hybrid Full Adder-20 Transistor

The above figure shows the schematic of hybrid full adder -20 transistors which is combination of number of PMOS and NMOS logic is designed in 65nm technology. It is designed with TannerS-EDIT Tool.

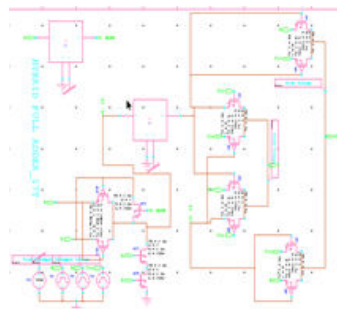


Figure 2: Simulation Of Hybrid Full Adder-20 Transistor

the above figure shows the PDP analysis of Hybrid Full Adder-20 Transistor. It analyzed by using Tanner tool. The PDP is 340.98. For above simulation have done with 0.8VDD.

The signal A, B are given to P4, P3. The transistor P4 is connected P5. The signal B is given to N3 and P5. The signal A is given to N3 and N4. The signal A is given to P6 and P7. The signal B is given to P7 and N5. The transistor N5 is connected N6. The signal B is connected N6 and the signal A is connected to N7. The output of P5 and N5 is Abar. The output of N3 and N4 is given N8, P9, N10 and P11. The output of P6 and P7 is given to P10, N11, P8 and N9. The signal Abar is given to P8 and N8. The signal Ci is given to P9 and N9.

The signal Ci is given to N10 and P10. The signal Ci is given to N11 and P11. The output of N9, P9 and N10, P10 are shorted together and is given to inverter which consist of P12 and N12, the output of inverter is sum. The output of N8, P8 and N11, P11 are shorted together and is given to inverter which consist of N13 and P13, the output of inverter is carry. The circuit is simulated in 65nm technology and result are obtained.

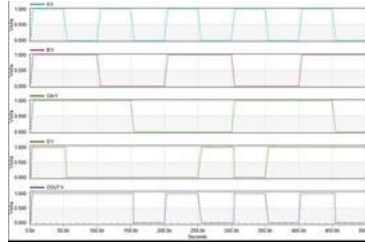


Figure 3: Simulation of Hybrid Full Adder-17 Transistor

The above figure shows the schematic of hybrid full adder 17 transistors which is a combination of number of PMOS and NMOS logic is designed in 16 nm technology. It is designed with Tanner S-EDIT Tool.

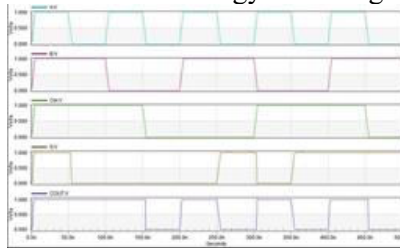


Figure 4: Simulation of Hybrid Full Adder 17 Transistor

The above figure shows the simulation results of Hybrid Full Adder 17 T Transistor. It is simulated using CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool. Waveforms are analyzed using W-EDIT (waveform editor).

The above figure shows the PDP analysis of Hybrid Full Adder 17 T Transistor. It is analyzed by using Tanner tool. The PDP is 291.1505. For the above simulation, we have done with 5 VDD.

The signals A and B are given to P4 and P3. The transistor P4 is connected to P5. The signal B is given to N3 and P5. The signal A is given to N3 and N4. The signal A is given to P6 and P7. The signal B is given to P7 and N5. The transistor N5 is connected to N6. The signal B is connected to N6 and the signal A is connected to N7. The output of P5 and N5 is A-bar. The output of N3 and N4 is given to N8, P9, N10, and P11. The output of P6 and P7 is given to P10, N11, P8, and N9. The signal A-bar is given to an inverter which consists of P12 and N12.

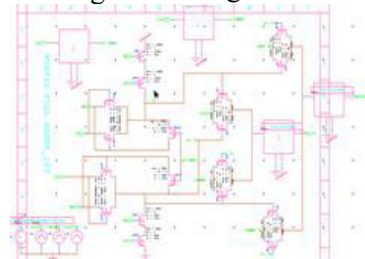


Figure 5: Schematic of Hybrid Full Adder-B-26 Transistor

The above figure shows the schematic of hybrid full adder-B-26 transistors which is a combination of number of PMOS and NMOS logic is designed in 65 nm technology. It is designed with Tanner S-EDIT Tool. The above figure shows the simulation results of Hybrid Full Adder-B-26 Transistor. It is simulated using CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool. Waveforms are analyzed using W-EDIT (waveform editor).

The signals A and B are given to P4 and P3. The transistor P4 is connected to P5. The signal B is given to N3 and P5. The signal A is given to N3 and N4. The signal A is given to P6 and P7. The signal B is given to P7 and N5. The transistor N5 is connected to N6. The signal B is connected to N6 and the signal A is connected to

N7. The output of P5 and N5 is Abar. The output of N3 and N4 is given to N8, P9, N10 and P11. The output of P6 and P7 is given to P10, N11, P8 and N9. The signal Abar is given to inverter which consists of P12 and N12.

The signal A, B are given to P4, P3. The transistor P4 is connected to P5. The signal B is given to N3 and P5. The signal A is given to N3 and N4. The signal A is given to P6 and P7. The signal B is given to P7 and N5. The transistor N5 is connected to N6. The signal B is connected to N6 [2] and the signal A is connected to N7. The output of P5 and N5 is Abar. The output of N3 and N4 is given to N8, P9, N10 and P11. The output of P6 and P7 is given to P10, N11, P8 and N9. The signal Abar is given to P8 and N8. The signal C is given to P9 and N9. The signal C is given to N10 and P10. The signal C is given to N11 and P11. The output of N9, P9 and N10, P10 are shorted together and is given to inverter which consists of P12 and N12, the output of inverter is sum. The output of N8, P8 and N11, P11 are shorted together and is given to inverter which consists of P13 and N13, the output of inverter is carry. The circuit is simulated in

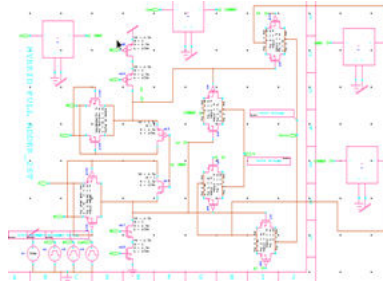


Figure 6: Schematic of Hybrid Full Adder HFA-NB-26T.

The above figure shows the schematic of hybrid full adder-B-26 transistors [3] which is a combination of number of PMOS and NMOS logic is designed in 65nm technology. It is designed with Tanner S-EDIT Tool

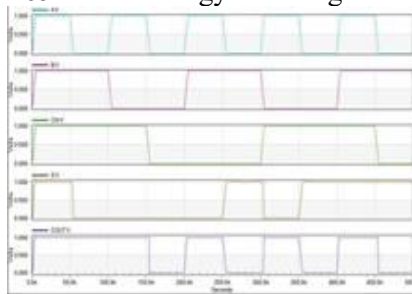


Figure 7: Simulation of Hybrid Full Adder-B-26 Transistor.

The above figure shows the simulation results of Hybrid Full Adder-B-26 Transistor. It is simulated using CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool. Wave forms are analyzed using W-EDIT (wave form editor). The signal A, B are given to P4, P3. The transistor P4 is connected to P5. The signal B is given to N3 and P5. The signal A is given to N3 and N4. The signal A is given to P6 and P7. The signal B is given to P7 and N5. The transistor N5 is connected to N6. The signal B is connected to N6 and the signal A is connected to N7. The output of P5 and N5 is Abar. The output of N3 and N4 is given to N8, P9, N10 and P11. The output of P6 and P7 is given to P10, N11, P8 and N9. The signal Abar is given to inverter which consists of P12 and N12.

The signal A, B are given to P4, P3. The transistor P4 is connected to P5. The signal B is given to N3 and P5. The signal A is given to N3 and N4. The signal A is given to P6 and P7 [4]. The signal B is given to P7 and N5. The transistor N5 is connected to N6. The signal B is connected to N6 and the signal A is connected to N7. The output of P5 and N5 is Abar. The output of N3 and N4

is given N8,P9,N10 and P11. The output of P6 and P7 is given to P10, N11, P8 and N9. The signal B is given to P8. The signal A is given to N8. The signal C_i is given to P9 and N9. The signal C_i is given to N10 and P10. The signal C_i is given to N11 and P11. The output of N9, P9 and N10, P10 are shorted together and the output is sum. The output of N8, P8.

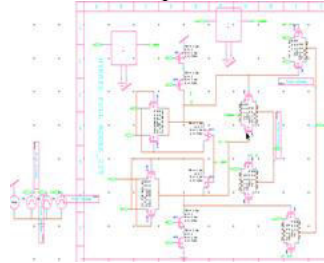


Figure 8: Simulation of Hybrid Full Adder HFA- 22T

The above figure shows the schematic of hybrid full adder -22 transistors which is a combination of number of PMOS and NMOS logic is designed in 65nm technology. It is designed with Tanner-EDIT Tool.

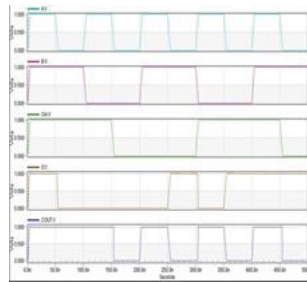


Figure 9: Simulation of Hybrid Full Adder-22 Transistor

The above figure shows the simulation results of Hybrid Full Adder-22 Transistor. It is simulated using CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool. Waveforms are analyzed using W-EDIT (waveform editor).

The input signal A is given to inverter which consists of P1 and N1 transistors. Carry signal C_i is given to inverter which consists of P2 and N2 transistor [5]. The signal A is given to P3, P2 and signal B is given to P2, N4. The output of P3, P2 are shorted together and is given to N4, the N4 is connected to N3. The signal A is given to N3 and signal B is given to N2. The output of P3, P2 is given to inverter which consists of P4 and N5. The output of inverter is given to N6, N7, N8, P7.

The signal C_i is given to N6, P5, N7, P6, N9, P7. The input of inverter is given to P6, P5, N9 and P8. The output of transistors N6, P5 and N7, P6 are shorted together. The output is sum. The output of N8, N7 and N9, P8 are shorted together and the output is carry. The circuit is simulated in 65nm technology and results are obtained.

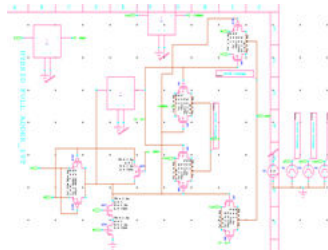


Figure 10: Simulation of Hybrid Full Adder HFA-19T

The above figure shows the schematic of hybrid full adder -19 transistors which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tannerS-EDIT Tool.

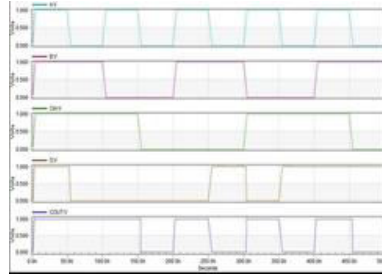


Figure 11: Simulation of Hybrid Full Adder-19 Transistor

The above figure shows the simulation results of Hybrid Full Adder-17 Transistor. It is simulated using CMOS Tanner-SPIICE[6](Simulation Program with Integrated Circuit Emphasis) Tool. Waveforms are analyzed using W-EDIT (waveform editor).

III. PROPOSED METHOD

For computational arithmetic, a full adder is the primary logic units in VLSI applications. A new full adder circuit design has been presented in this article which is based on input switching activity pattern and gate diffusion input (GDI) technique.[7] The adder has been designed in two stages. The first stage is an XOR–XNOR module, whereas, the final stage is for the required outputs. By using the switching activity pattern of inputs and GDI techniques at each stage, the switching activities of the transistors have been minimized. This improves delay, power consumption and computational complexity. The adder has been designed and evaluated by using the synopsis tool and compared with different existing adder cells found in the literature. It is found that the presented adder shows an improvement at least 72.86% and 66.67% in terms of speed and energy consumption, respectively. Extensive performance analyses of the full adder have also been evaluated at 16 nm technology node which shows promising performances in both the technology nodes. Summarily, the main contributions of the proposed work are listed below:

1. A 1-bit full adder circuit has been designed for VLSI applications based on switching activity and GDI technique which is compatible both with CMOS and CNFET technology.
2. The circuit has been designed in two stages. In the first stage, an XOR–XNOR [8] module has been designed, whereas, in the second stage
3. the sum and carry modules have been designed. The overall circuit requires only 10 transistors.
4. By utilizing the switching activity pattern of the inputs and GDI techniques at each stage, the switching activities of the transistor (transitions) have been minimized during data flow from input to the outputs which ensures less delay and low power consumption.
5. Moreover, as C_{in} is introduced at the final stage, the initial circuit operation becomes independent of C_{in} that helps in further reduction in delay.
6. The simulations and analysis have been carried out in 90 nm CMOS, 32 nm CMOS and 32 nm technology nodes.
7. A comparative analysis has been carried out comprehensively to establish the utility of the proposed design.

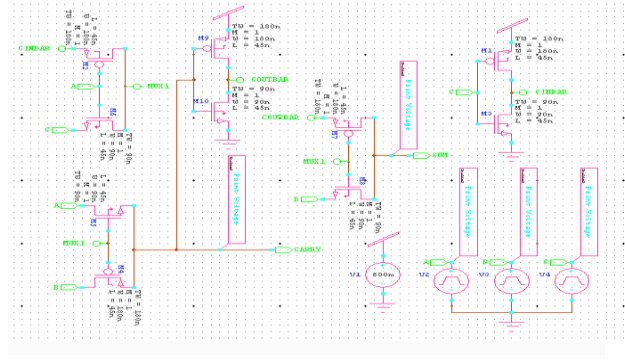


Figure 12: Simulation of Hybrid Full Adder-10 Transistor

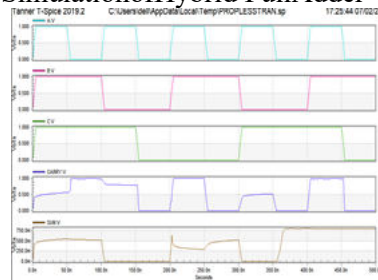


Figure 13: Simulation of Hybrid Full Adder-10 Transistor

The above figure shows the simulation results of Hybrid Full Adder-17 Transistor. It is simulated using CMOS Tanner SPICE (Simulation Program with Integrated Circuit Emphasis) Tool. Waveforms are analyzed using W-EDIT (waveform editor).

IV. CONCLUSION

We initially assessed XOR-XNOR schematics in this project. The simulation demonstrates that the circuit's NOT gates are a drawback, and positive feedback is another drawback. The latency, output capacitance, and power consumption all rise as a result of the feedback [9]. Next, we suggest novel XOR-XNOR designs that might not have the drawbacks mentioned above. For different algorithms, we created three new FA circuits employing the suggested XOR-XNOR gates. The results of simulating FA circuits under various settings demonstrate that the suggested designs function exceptionally well across the board. According to simulation studies, compared to previous FA [10] circuit designs, the suggested FA schematics save PDP by up to 23%. The suggested FA designs are the fastest and most powerful.

A. FUTURE SCOPE

In high-performance digital systems like microprocessors, digital signal processors (DSPs), and other applications, the requirement for low power design is increasingly becoming a significant problem. Very complicated chips with high clock frequencies are designed as a result of increasing chip density and operating speed. In high-end systems with high integration densities, low power design is also necessary to lower power consumption and increase operating speed.

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