# OPTIMIZED VLSI DESIGN FOR CONVOLUTIVE BLIND SOURCE SEPARATION APPLICATIONS

*[1]GANESH URUGONDA,[2]VEERAMALLA SUMALINI,[3]RANGAREE HIVRAJ PANKAJ, [4]CHERUKUPELLI SUPRIYA,[5]CHIRRA SINDHU*
*[123]Assistant Professor,[45]Students*
*Department of ECE*
*Vaagdevi College of Engineering, Warangal, Telangana*

**ABSTRACT:**
A basic signal processing method utilised in many fields, such as image, audio, and biological signal processing, is blind source separation (BSS). Convolutive BSS is a particularly difficult problem since it aims to separate mixed sources while the mixing process is described by convolution. In order to satisfy the requirements of real-time and effective processing in applications including echo cancellation, audio source separation, and speech enhancement, this study presents a unique VLSI (Very Large Scale Integration) architecture designed for convolutive blind source separation. The suggested VLSI architecture achieves complicated BSS with low latency and high accuracy by utilising cutting-edge hardware innovations and algorithms. It combines many processing components, each of which is in charge of locating and isolating the distinct source signals from the mixture being monitored. These processing components improve separation performance even when dealing with time-varying mixture circumstances by iteratively refining source estimations using advanced signal processing and adaptive filtering approaches. Memory-efficient data structures, adaptive parameter tuning, and parallel processing units are crucial elements of the VLSI architecture. Because it can handle varying input volumes and adapt to various processing needs, it is appropriate for a variety of real-world applications. The experimental findings show that the suggested VLSI design is efficient and effective in convolutive BSS conditions. It also shows that it can separate mixed sources in real time with high-quality signals. The hardware architecture is a useful tool for signal processing systems that must extract significant source information from complicated mixes because to its scalability and durability.
**Keywords:** high efficiency, memory, VLSI, and BSS.

## I.INTRODUCTION

A crucial signal processing method, blind source separation (BSS) has several uses in industries including biomedical engineering, telecommunications, and audio processing, among others. In situations when the mixing process is unknown beforehand, it entails the separation of signals from mixed sources. Convolutive blind source separation is a very intricate and difficult variation of BSS in which sources are combined by convolution to mimic real-world situations such as acoustic settings with numerous sound sources and reflections. Applications like acoustic echo cancellation, audio source separation, and speech improvement, among many others, have made convolutive BSS extremely important. The time-varying aspect of the mixing process creates special difficulties since real-time separation necessitates complex algorithms and effective hardware implementations. In order to overcome the difficulties presented by convolutive BSS, a specialised Very Large Scale Integration (VLSI) architecture is developed in this study. For convolutive BSS systems that need both precision and real-time capabilities, VLSI architecture is the perfect platform since it makes it possible to execute complicated signal processing tasks quickly and efficiently. Presenting a unique VLSI architecture suited to convolutive BSS situations is the goal of this article. To effectively separate mixed sources, this architecture makes use of memory-efficient data structures, adaptive parameter tuning, parallel processing components, and sophisticated signal processing algorithms. The suggested VLSI design aims to meet the urgent need for high-performance BSS solutions in a variety of real-world applications by using these qualities to enable the real-time isolation of sources from complex mixes. We shall examine the VLSI architecture for convolutive blind source separation's architectural specifics, computational strategies, and experimental outcomes in the sections that follow. The possibilities and potential influence of this VLSI approach in developing signal processing systems, especially in situations requiring convolution-based mixing, will be fully understood by readers by the conclusion of this study.

In situations when the majority of the information regarding sources and mixed signals is unknown, blind source separation is a type of filtering technique used to separate distinct sources from the signals. Blind source separation is a difficult undertaking because of this limitation. In several domains, including image processing, communication systems, biomedical signal processing, and audio signal processing, blind source separation becomes a crucial study problem. Instantaneous mixing without a filtering effect is referred to as a simple mixing procedure. Before reaching the microphones, the audio source should undergo a complex mixing process that passes through a filtering environment. The original audio source should then be recovered using convoluted blind source separation. To handle the CBSS problem, one of the traditional approaches is independent component analysis (ICA). The main disadvantage of implementing software with this method is that it is frequently a more time-consuming and computationally demanding procedure. Since the hardware method provides ideal parallelism, there has been a lot of interest in providing hardware solutions for ICA-based blind source separation. Above-and-sub-threshold CMOS circuit design approaches may be used to create an analogue BSS chip that incorporates an analogue i/o interface, weight coefficients, and adoption blocks.

## II. LITERATURE SURVEY

Separating brain imaging signals by maximizing their autocorrelations is an important component of blind source separation (BSS). Canonical correlation analysis (CCA), one of leading BSS techniques, has been widely used for analyzing optical imaging (OI) and functional magnetic resonance imaging (fMRI) data. However, because of the need to reduce dimensionality and ignore spatial autocorrelation, CCA is problematic for separating temporal signal sources. To solve the problems of CCA, "straightforward image projection" (SIP) has been incorporated into temporal BSS. This novel method, termed low-dimensional canonical correlation analysis (LD-CCA), relies on the spatial and temporal autocorrelations of all genuine signals of interest. Incorporating both spatial and temporal information, here we introduce a "generalized timecourse" technique in which data are artificially reorganized prior to separation. The quantity of spatial plus temporal autocorrelations can then be defined. By maximizing temporal and spatial autocorrelations in combination, LD-CCA is able to obtain expected "real" signal sources. Generalized timecourses are low-dimensional, eliminating the need for dimension reduction. This removes the risk of discarding useful information. The new method is compared with temporal CCA and temporal independent component analysis (tICA). Comparison of simulated data showed that LD-CCA was more effective for recovering signal sources. Comparisons using real intrinsic OI and fMRI data also supported the validity of LD-CCA. Online blind source separation (BSS) is proposed to overcome the high computational cost problem, which limits the practical applications of traditional batch BSS algorithms. However, the existing online BSS methods are mainly used to separate independent or uncorrelated sources.

Recently, nonnegative matrix factorization (NMF) shows great potential to separate the correlative sources, where some constraints are often imposed to overcome the non uniqueness of the factorization. In this paper, an incremental NMF with volume constraint is derived and utilized for solving online BSS. The volume constraint to the mixing matrix enhances the identifiability of the sources, while the incremental learning mode reduces the computational cost. The proposed method takes advantage of the natural gradient based multiplication updating rule, and it performs especially well in the recovery of dependent sources. Simulations in BSS for dual-energy X-ray images, online encrypted speech signals, and high correlative face images show the validity of the proposed method. This brief presents an efficient verylarge-scale integration architecture design for convolutive blind source separation (CBSS). The CBSS separation network derived from the information maximization (Infomax) approach is adopted. The proposed CBSS chip design consists mainly of Infomax filtering modules and scaling factor computation modules. In an Infomax filtering module, input samples are filtered by an Infomax filter with the weights updated by Infomax-driven stochastic learning rules. As for the scaling factor computation module, all operations including logistic sigmoid are integrated and implemented by the circuit design based on a piece wise linear approximation scheme.

## III. PROPOSED SYSTEM

A proposed system for VLSI Design for Convolutive Blind Source Separation would involve the development of a specialized hardware architecture capable of efficiently and accurately separating mixed sources in real-time, particularly in scenarios where the mixing process is described by convolution. Here's an overview of the key components and features that such a system might include:

DOI:10.48047/intjecse/v13i2.21285 ISSN: 1308-5581 Vol 13, Issue 02 2021

**1. Hardware Architecture:** The core of the proposed system is a custom-designed VLSI architecture optimized for convolutive blind source separation. This architecture would consist of dedicated hardware modules and processing units tailored to perform the necessary signal processing tasks efficiently.
**2. Parallel Processing:** To handle the computational demands of convolutive BSS in real-time, the VLSI system would incorporate parallel processing units. These units would enable simultaneous processing of multiple data streams, accelerating the separation process.
**3. Adaptive Filtering:** Advanced adaptive filtering algorithms would be implemented in hardware to estimate and separate the individual source signals. These algorithms should be capable of adapting to changing mixing conditions, making the system robust in real-world scenarios.
**4. Memory Management:** Efficient memory management is essential to store intermediate results and filter coefficients. The system should include memory units optimized for low-latency access to data.
**5. Parameter Tuning:** The architecture may incorporate adaptive parameter tuning mechanisms that automatically adjust filter coefficients and other parameters based on the characteristics of the input signals and the mixing environment.
**6. Real-Time Processing:** Real-time performance is crucial for applications like audio source separation and speech enhancement. The proposed system should be capable of processing incoming data streams with low latency.
**7. Scalability:** The system's architecture should be scalable to accommodate different numbers of sources and adapt to varying computational requirements.
**8. Noise Reduction:** To enhance the quality of separated signals, noise reduction techniques may be integrated into the system, especially in noisy environments.
**9. Evaluation and Testing:** The proposed system would undergo extensive testing and evaluation to validate its performance in various scenarios. Metrics such as Signal-to-Noise Ratio (SNR) and Separation Quality Metrics may be used for evaluation.
**10. Integration:** The VLSI system should be designed for easy integration into larger signal processing systems or devices, such as audio processors, medical equipment, or communication systems.
**11. Energy Efficiency:** To make the system suitable for portable and battery-powered devices, energy-efficient hardware design should be a consideration.
**12. Algorithm Flexibility:** While the focus is on convolutive BSS, the system may be designed to accommodate different blind source separation algorithms, offering flexibility for various applications.

The proposed system aims to provide an efficient and versatile solution for convolutive blind source separation, addressing the challenges posed by real-time processing, changing mixing conditions, and the need for high-quality source separation. It has the potential to enhance various applications, including speech enhancement, audio source separation, biomedical signal processing, and more.

## IV. METHODOLOGY

The proposed CBSS system is shown in the FIG. The CBSS chip mainly consists of two functional cores: Infomax filtering module and scaling factor computation module. Additionally, the Infomax filtering outputs are added with the help of two small carry-save adders (CSAs). The current prototype chip is used for two sources and two sensors by utilizing four Infomax filtering modules along with two scaling factor computation modules.

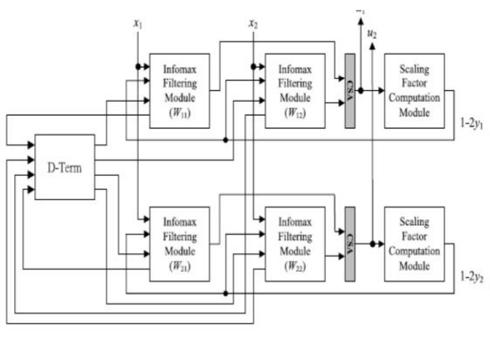
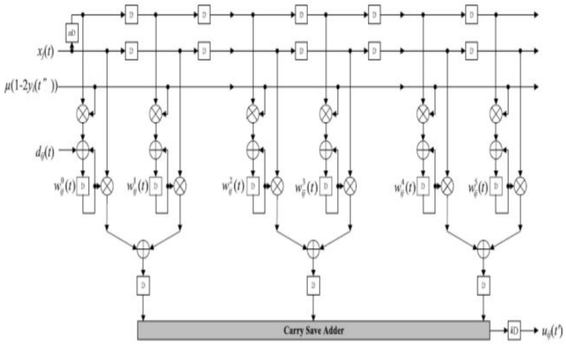



**Fig.1. Proposed model.**

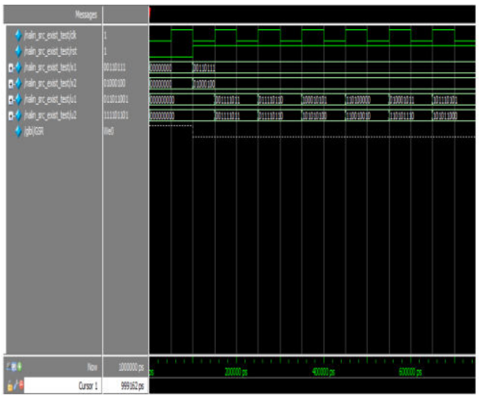
The Infomax filtering module for the proposed system is shown in fig.3. In the fig. 1, the CBSS separation network contains four causal FIR filters. These filters are adaptive because stochastic learning rules which are derived from the Infomax approach will alter the tap coefficients and are thus referred to herein as the

DOI:10.48047/intjecse/v13i2.21285 ISSN: 1308-5581 Vol 13, Issue 02 2021

Infomax adaptive filter or the Infomax filter. The Infomax filtering module is exemplified with six taps. In the Infomax filtering module, an input sample passes through lower and upper register chains. These samples are multiplied with filter weights and scaling factors, respectively. The multiplication results of all of the taps are accumulated by a two-stage summation. The first stage adopts carry lookahead adders to generate the intermediate addition results for multiplication of every two successive taps. The above intermediate addition results are summed up by using a carry save addition scheme. A CSA(carry save adder) can accept more than two data inputs.




According to our numerical analysis, five line segments are sufficient to approximate with a negligible error. Let lsi, i = 1, 2, . . . , 5 denote the ith line segment, and ci represent the connected point between two consecutive line segments. To implement the line-segment approximation, the circuit design for scaling factor computation is to calculate single variable linear equations. For the equation of lsi which corresponding to mi(n) = ai n + bi, i = 1, 2, . . . , 5, where n = ui(t). As the slopes of ls1 and ls5 are the same, these two line segments share the equation parameters a1. In the same manner, line segments ls2 and ls4 share the equation parameters a2. Furthermore, according to the symmetry in Fig. 5, the bias used for line segment ls5, e.g., −b1, is the negative of the bias b1 used for line segment ls1. In addition, line segments ls4 and ls2 use biases −b2 and b2, respectively .As for the d0 ij(t) , this study designs a Dterm unit to execute dij(t) = cofactor(wij)(detW0) -1. The architecture of the D-term unit is shown in Fig. The Dterm unit consists of a determinant circuit to find.



## V. CONCLUSION

For a while now, CBSS has used this quick VLSI design method. A design based on the Info-max filtering system and scaling aspect calculation modules are used to calculate CBSS separation networks. Utilising TSMC's state-of-the-art 90-nm CMOS technology, the proposed ASIC device has a die size of about 0.54 mm2 by 0.54 mm2. With a power consumption of only 54.86 mW, 100 MHz is the ideal operating voltage for a 1.8-V power supply. In addition to being utilised for reprocessing, the suggested CBSS ASIC chip may be integrated with additional sound processing chips and auxiliary parts to create a comprehensive sound processing system.

## REFERANCES

[1] G. Zhou, Z. Yang, S. Xie, and J. M. Yang, "Online blind source separation using incremental nonnegative matrix factorization with volume constraint," IEEE Trans. Neural Netw., vol. 22, no. 4, pp. 550–560, Apr. 2011.

[2] M. Li, Y. Liu, G. Feng, Z. Zhou, and D. Hu, "OI and fMRI signal separation using both temporal and spatial autocorrelations," IEEE Trans. Biomed. Eng., vol. 57, no. 8, pp. 1917–1926, Aug. 2010.
[3] A. Tonazzini, I. Gerace, and F. Martinelli, "Multichannel blind separation and deconvolution of images for document analysis," IEEE Trans. Image Process., vol. 19, no. 4, pp. 912–925, Apr. 2010.
[4] H. L. N. Thi and C. Jutte, "Blind source separation for convolutive mixtures," Signal Process., vol. 45, no. 2, pp. 209–229, Aug. 1995.
[5] A. J. Bell and T. J. Sejnowski, "Blind separation and blind deconvolution: An information-theoretic approach," in Proc. Int. Conf. Acoust., Speech, Signal Process., May 1995, vol. 5, pp. 3415–3418.
[6] A. Hyvärinen and E. Oja, "Independent component analysis: Algorithms and applications," Neural Netw., vol. 13, no. 4/5, pp. 411–430, May/Jun. 2000.
[7] M. H. Cohen and A. G. Andreou, "Analog CMOS integration and experimentation with an autoadaptive independent component analyzer," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 42, no. 2, pp. 65– 77, Feb. 1995.
[8] K. S. Cho and S. Y. Lee, "Implementation of InfoMax ICA algorithm with analog CMOS circuits," in Proc. Int. Workshop Independent Compon. Anal. Blind Signal Separation, Dec. 2001, pp. 70–73.
[9] Z. Li and Q. Lin, "FPGA implementation of Infomax BSS algorithm with fixed-point number representation," in Proc. Int. Conf. Neural Netw. Brain, 2005, vol. 2, pp. 889–892.
[10] H. Du and H. Qi, "An FPGA implementation of parallel ICA for dimensionality reduction in hyperspectral images," in Proc. IEEE Int. Geosci. Remote Sens.Symp., Sep. 2004, pp. 3257–3260.
[11] M. Ounas, R. Touhami, and M. C. E. Yagoub, "Low cost architecture of digital circuit for FPGA implementation based ICA training algorithm of blind signal separation," in Proc. Int. Symp. Signals, Syst. Electron., 2007, pp. 135– 138.
[12] K. K. Shyu, M. H. Lee, Y. T. Wu, and P. L. Lee, "Implementation of pipelined FastICA on FPGA for real-time blind source separation," IEEE Trans. Neural Netw., vol. 19, no. 6, pp. 958–970, Jun. 2008.